THE ANALYSIS OF DEAD TIME VARIATION ON SWITCHING LOSS IN HIGH AND LOW SIDE MOSFETS OF ZVS SYNCHRONOUS BUCK CONVERTER CIRCUIT

By

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FINAL REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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Approved:

_____

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Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

December 2009

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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Michelle Lee Kim Xin

ABSTRACT

This work is about the analysis of dead time variation on switching losses in a Zero Voltage Switching (ZVS) synchronous buck converter (SBC) circuit. In high frequency converter circuits, switching losses are commonly linked with high and low side switches of SBC circuit. They are activated externally by the gate driver circuit. The duty ratio, dead time and resonant inductor are the parameters that affect the efficiency of the circuit. These variables can be adjusted for the optimization purposes. The study primarily focuses on varying the settings of input pulses of the MOSFETs in the resonant gate driver circuit which consequently affects the efficiency of the ZVS synchronous buck converter circuit. Using the predetermined inductor of 9 nH, the frequency is maintained at 1 MHz for each cycle transition. This work has given positive sign of improvement. The switching loss graph is obtained and switching losses for both S_1 and S_2 are calculated and compared to the findings from [1]. It has shown a decrease in losses by 12.1 % in S_1 and 31.8 % in S_2, respectively.

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LIST OF ABBREVIATIONS

SBC	Synchronous Buck Converter
RGD	Resonant Gate Driver
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
DC-RGD	Diode Clamped Resonant Gate Driver

CHAPTER 1
INTRODUCTION

1.1 Background of Study

In high frequency synchronous buck converter (SBC) circuit where the range of high frequency is defined from 1 MHz to 30 MHz, main losses are normally caused by the high and low side switches. The resonant gate driver (RGD) circuit is chosen due to its suitability in driving MOS-gated power switches in high frequency applications. At present, there are various types of RGD circuits commercially available [2-4]. The resonant circuit transfers energy from the parasitic input capacitance of the power switching devices. This energy transfer prevents dissipation of the capacitive energy in the driver circuit which may otherwise destroy one or more components. The resonant circuit includes an inductor in the driver circuit and one or more discrete capacitors are also included within the driver circuit to maintain resonance at a given frequency regardless of parasitic capacitance variation [5].

High power Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is used as a switch in this work of the proposed RGD circuit [1]. Although high frequency MOSFET is used, yet there are limitations in the design. When the frequency is increased, the gate driving losses will experience an increase in power dissipation. This in turn affects the performance and efficiency of the converter. The duty ratio or pulse width, D, dead time, T_D, and the resonant inductor, L_r are the limiting parameters that affect the gate driver operation from conducting optimally. These parameters had been analyzed in [6] and the results show that the optimized values are found to be D = 20%, T_D = 15 ns and L_r = 9 nH at 1 MHz switching frequency. However, the values of switching losses in the MOSFET are still very high. Therefore, the T_D parameter is adjusted to optimize switching losses. This is the primary objective in this work.

1.2 Problem Statement

The implication of using MOSFET as a switch in RGD circuits operating at high frequency is the switching losses. In order to reduce the switching loses, one way is to modify the settings on 4 individual MOSFETs in the proposed RGD circuit. They have to be adjusted with respect to the value of T_D while other circuit parameter values are kept unchanged in this work. As a result, the performance of the circuit can be evaluated.

1.3 Objective and Scope of Study

The objective of the work is to improve the performance of converter circuit. This is done by decreasing the switching losses in the high and low side MOSFETs of the circuit. In order to achieve this objective, the pulse setting of the 4 MOSFETs in the proposed RGD circuit is modified carefully resulting in different values of T_D. The RGD circuit accordingly in turn affects the T_D of the synchronous buck converter circuit. Therefore, the switching losses of the circuit are measured at the two MOSFET switches of S_1 and S_2. The results are then measured, compared and analyzed.

CHAPTER 2
LITERATURE REVIEW

2.1 Converter Circuit

A power electronic converter is used to convert electrical power from one form to another. For example, DC-DC converters are widely used in battery chargers, DC motor drives, computer motherboard and many other electronic applications. The most common and basic converter's topologies are:

a. step-down (buck) converter
b. step-up (boost) converter, and
c. step-down / step-up (buck-boost) converter.

2.2 Synchronous Buck Converter Circuit

A buck converter circuit is a step-down converter which produces a lower output voltage than the DC input voltage. Figure 1 below shows a buck converter circuit.

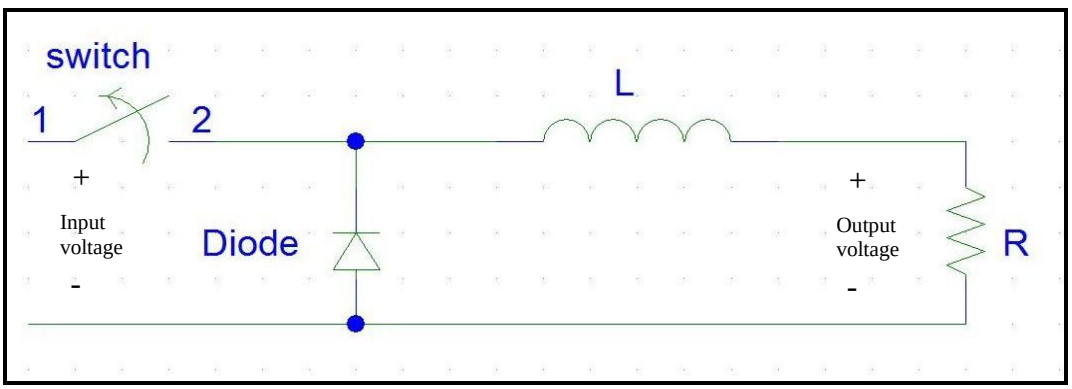


Figure 1 Buck Converter Circuit

In a buck converter, the freewheeling diode turns on, on its own, shortly after the switch turns off, as a result of the rising voltage across the diode. This voltage drop across the diode results in a power loss defined by (1)

$$P_D = V_D \bullet (1-D) \bullet I_o \tag{1}$$

where P_D = power loss of diode

V_D = voltage drop across diode

D = duty ratio

I_o = load current

A synchronous buck converter on the other hand is a modified version of the basic buck converter circuit topology in which the diode is replaced with a second switch, S_2. This modification is a tradeoff between increased cost and improved efficiency. Figure 2 shows the synchronous buck converter circuit.

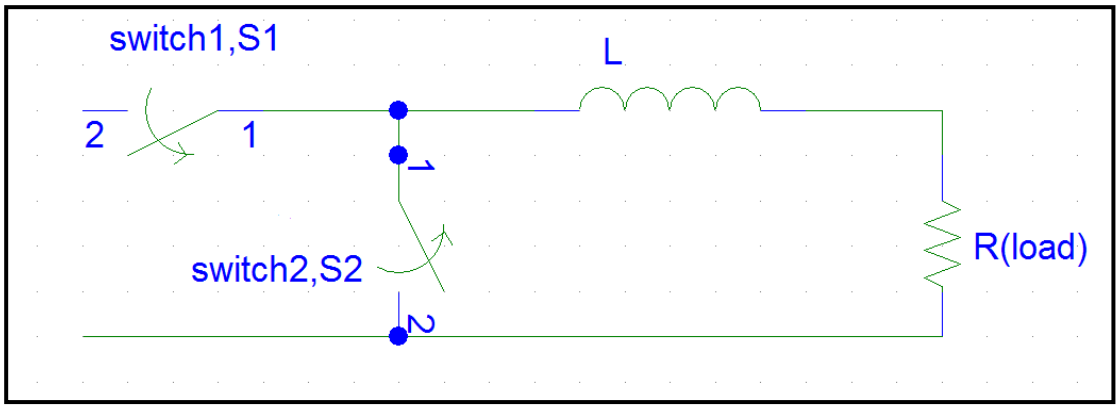


Figure 2 Synchronous Buck Converter Circuit

By replacing the diode with switch, S_2, which is advantageously selected for low losses, the converter efficiency can be improved. The providing power loss on switch, S_2 would be defined by (2)

$$P_{s2} = I_o^{\,2} \bullet R_{DSon} \bullet (1 - D) \tag{2}$$

where P_{s2} = power loss on switch, S_2

R_{DSon} = resistance of switch (i.e. MOSFET)

Comparing both equations (1) and (2), it can be seen that power loss is strongly dependent on the duty ratio, *D*. It stands to reason that the power on the second switch will be proportional to its on-time.

An advantage of the synchronous converter is that it is bi-directional, which lends itself to applications requiring regenerative braking. When power is transferred in the "reverse" direction, it acts much like a boost converter instead.

Alas, the advantage of this converter does not come without cost. Firstly, the lower switch typically costs more than the freewheeling diode in the basic buck converter circuit. Secondly, the complexity of the converter is vastly increased due to the need for a complementary-output switch driver. Therefore, the RGD circuit is used.

2.3 Time Translation or Dead Time

In the synchronous buck circuit, the dead time is shown in Figure 3. The switches can be MOSFETs, Insulated Gate Bipolar Transistor (IGBT), Gate Turn-off Thyristors (GTO) or other ideal switches.

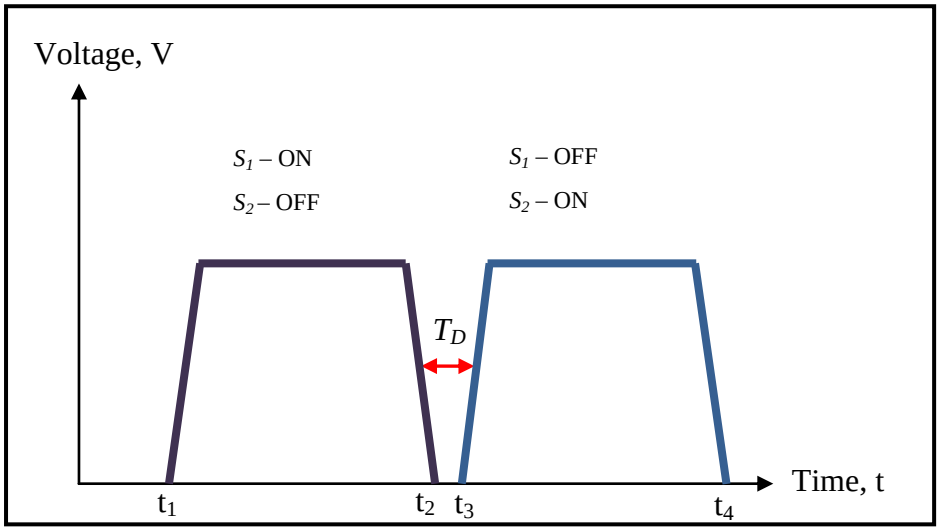


Figure 3 Dead time, T_D

Switch 1, S_1 and Switch 2, S_2 conduct complimentarily to produce the waveform as shown in Figure 3. The time in between when both switches are off is the dead time, T_D.

2.4 Duty ratio, *D*

The duty ratio or duty cycle is defined as D [5] and it is represented by (3)

$$D = \frac{t_{on}}{t_{on} + t_{off}}$$

$$D = \frac{t_{on}}{T_s} \tag{3}$$

where t_{on} = on time of the ideal switch

t_{off} = off time of the ideal switch

T_s = switching period

From Figure 3, it can be observed that switch 1, S_1 turns on from t_1 to t_2, while switch 2, S_2 is turned off during this period of time. On the other hand, S_2 turns on from t_3 to t_4, while S_1 is turned off. To calculate the duty ratio of S_1 and S_2, we use the formula represented by (4) and (5)

$$\text{Duty ratio for } S_1,\ D_{S1} = \frac{t_2 - t_1}{t_4 - t_1} \tag{4}$$

$$\text{Duty ratio for } S_2,\ D_{S2} = \frac{t_4 - t_3}{t_4 - t_1} \tag{5}$$

2.5 Conventional Gate Driver Circuit, Diode Clamped Resonant Gate Driver (DC-RGD) circuit and the Proposed RGD Circuit

The conventional gate driver circuit and DC-RGD are shown in Figure 4 and Figure 5.

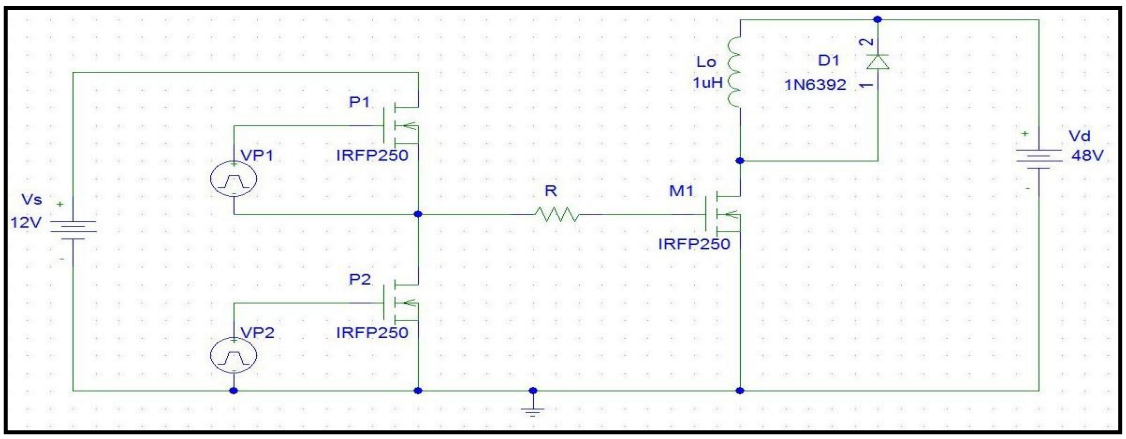


Figure 4 Conventional Gate Driver Circuit

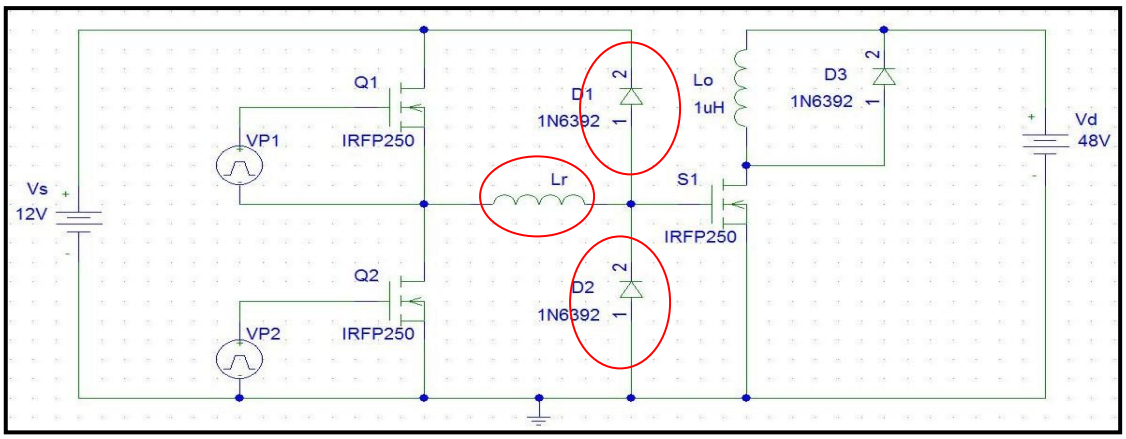


Figure 5 DC-RGD Circuit

The difference between the two circuits above is that in DC-RGD circuit, the resistor, R is replaced with resonant inductor, L_r and diodes, D_1 and D_2 are added. The disadvantage of using the conventional circuit is that R provides high resistance to the circuit which limits gate current to M_1. In the conventional gate driver circuit, when P_1 is conducting, the input capacitance and the gate source voltage, V_{gs} of M_1 is charged while P_2 is off. After a period of time, P_2 turns on while P_1 stops conducting. The input capacitance of M_1 tends to charge and discharge the V_{gs} of M_1. Consequently, it causes the variation in charged and discharged current of R, I_R. This leads to high dissipation in R when frequency increases.

By implementing the DC-RGD circuit, the charging and discharging of inductance generates a resonant link between V_s and S_1. The resonant link basically introduces zero voltage or zero current intervals. Therefore, when DC-RGD is compared to the conventional gate driver circuit, more energy can be saved in the DC-RGD circuit. The switching losses in RGD circuit are high especially in the transistors, Q_1 and Q_2. These losses are caused by rapid switching transition in transistors when they turn on and off.

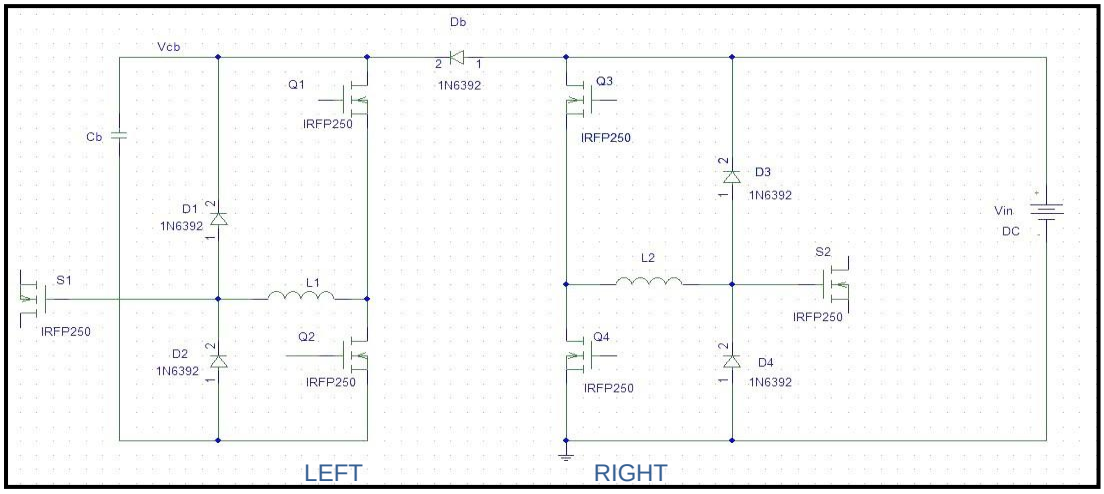


Figure 6 Proposed RGD Circuit

Figure 6 shows the proposed RGD circuit which is used in this work. The circuit is suitable for SBC circuit because with an input voltage, V_{in}, 2 output gate voltages will be generated complimentarily. Figure 7 shows the 2 output waveform generated from an input voltage of the SBC circuit.

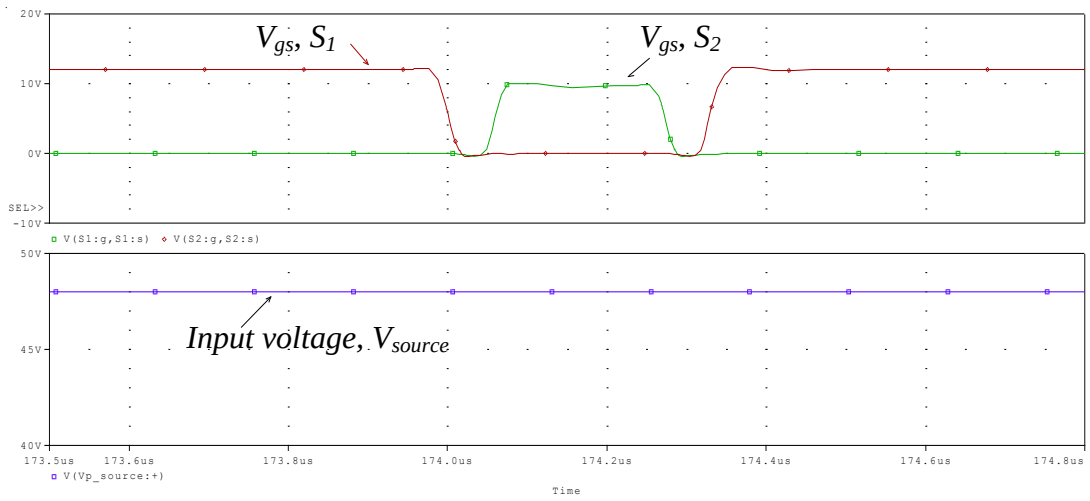


Figure 7 An input voltage generates 2 output gate voltages complimentarily in SBC circuit

As it can be seen, the left circuit of the proposed RGD circuit is the DC-RGD while the right circuit is just the symmetrical of the left circuit. The circuit has the advantages of simplification and symmetrical pattern which give better choice of component and parameter modification. In addition, a bootstrap circuit for high side drive [3] consisting of a diode, D_b and a capacitor, C_b are added into the circuit. The importance of bootstrap circuitry is that it aids in circuit simplification, symmetrical behavior and also minimizes switching loss. Besides that, it has less impact on the parasitic capacitance as well as better immunity in *dv/dt* turn-on. The proposed RGD circuit can conduct in two modes, complementary mode and symmetrical mode. In the complementary mode, it provides two drive signals with duty cycle D and 1-D, respectively. This mode is suitable for driving two MOSFETs in a synchronous buck converter.

In the circuit, the 4 units of MOSFETs (*Q1*, *Q2*, *Q3*, *Q4*) settings will be reassigned carefully whilst other values which include oscillation frequency = 1 MHz, D = 20% and L_r = 9nH remains unchanged. Theoretically, when parameters of MOSFETS, Q_1 and Q_2 of the RGD circuit are changed, dead time of the left circuit, T_{D1} will vary. Similarly, when parameter values of Q_3 and Q_4 are changed, then dead time of the right circuit, T_{D2} will be also be modified. Consequently, the overall value

of T_D in the proposed synchronous buck converter circuit as shown below in Figure 8 will also be modified. This results in new values of D and (1-D) in the synchronous buck circuit. S_1 is the high side switch while S_2 is the lower side switch and the switching losses of the circuit will be measured from these two switches. Overall, it is expected that the by varying the value of T_D, the performance of the SBC circuit will be affected, accordingly.

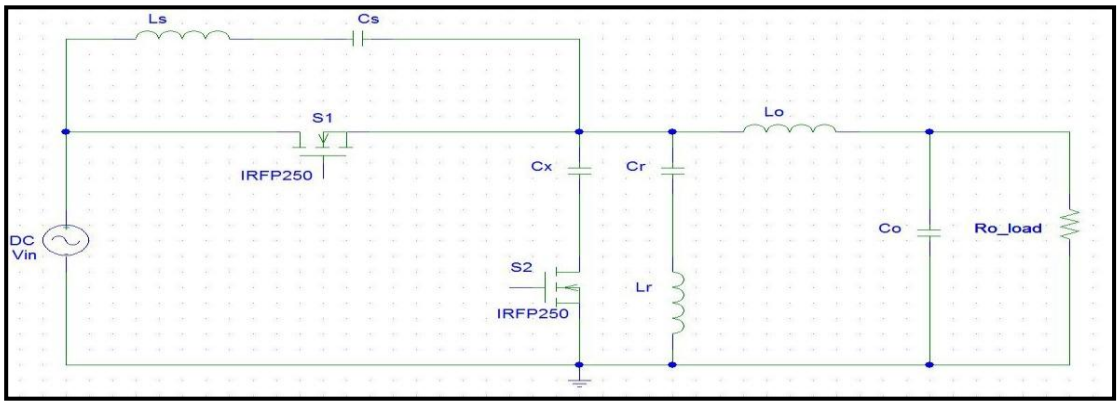


Figure 8 Proposed Synchronous Buck Converter Circuit with ZVS

When the values of switching frequency = 1 MHz and L_r = 9 nH, together with the optimized value of T_D are unchanged, and the value of D in the RGD circuit is altered instead, this will give new values of D and (1-D) in the synchronous buck circuit also. From this result, the switching losses and efficiency of the circuit can be observed and evaluated.

2.6 Series-resonant and parallel-resonant circuit

The configuration of inductor and capacitor connected together is a resonant circuit which acts as a filter to decrease the switching losses in the circuit. From the SBC circuit, several *LC* filter can be identified as shown in Figure 9.

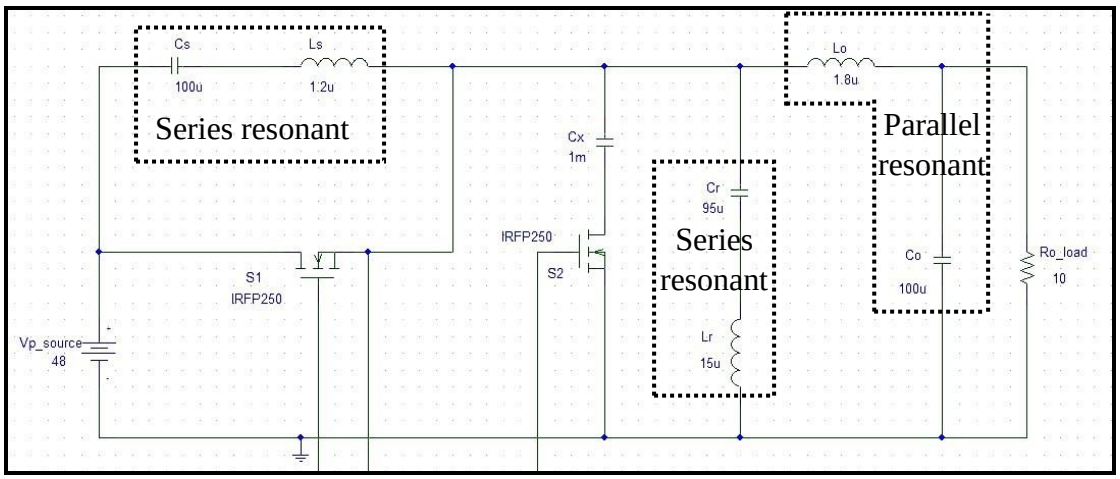


Figure 9 SBC circuit with identification of resonant circuits

There are mainly three types of resonant circuit; series resonant, parallel resonant and series-parallel resonant. An undamped series-resonant circuit is shown in Figure 10.

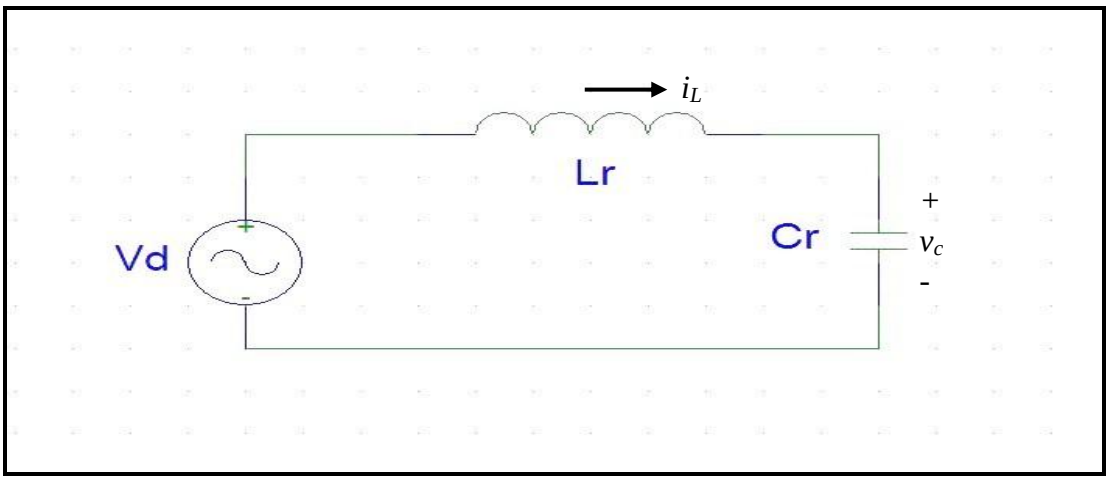


Figure 10 Undamped Series-Resonant Circuit

V_d is the input voltage while i_L is the inductor current and v_c is the capacitor voltage and I_{L0} and V_{c0} are intial conditions. The circuit equations are represented by (6) and (7)

$$L_r \frac{di_L}{dt} + v_c = V_d \tag{6}$$

and

$$C_r \frac{dv_c}{dt} = i_L \tag{7}$$

The solution of this set of equations for $t \geq t_0$ is represented by (8) and (9)

$$i_L(t) = I_{L0} \cos \omega_0 (t - t_0) + \frac{V_d - V_{c0}}{Z_o} \sin \omega_0 (t - t_0) \tag{8}$$

and

$$v_c(t) = V_d - (V_d - V_{c0}) \cos \omega_0 (t - t_0) + Z_o I_{L0} \sin \omega_0 (t - t_0) \tag{9}$$

where $\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}}$ is the angular resonance frequency

$Z_0 = \sqrt{\frac{L_r}{C_r}}$ Ω is the characteristic impedance

On the other hand, the undamped parallel-resonant circuit is shown in Figure 11.

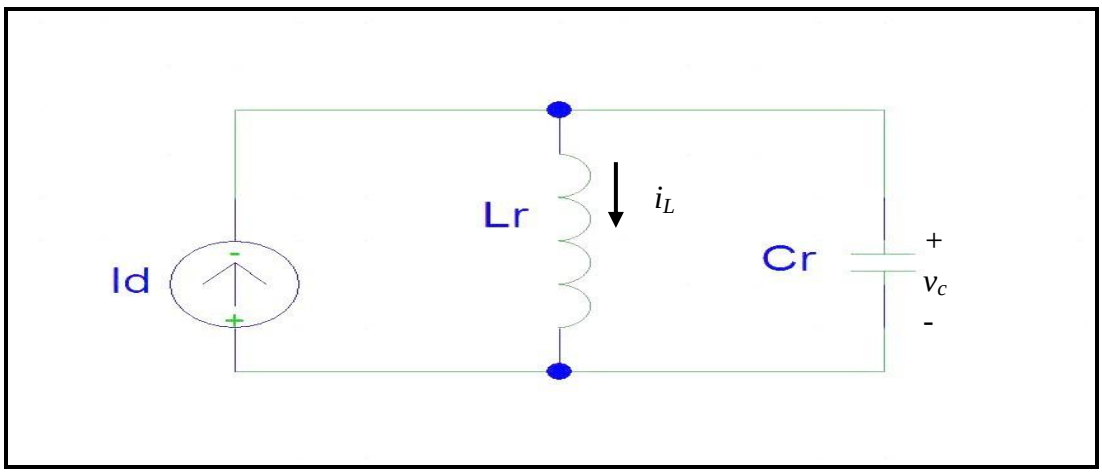


Figure 11 Undamped parallel-resonant circuit

The circuit is supplied by a DC current I_d. I_{L0} and V_{c0} are intial conditions at $t = t_0$. The circuit is represented by the equations (10) and (11)

$$i_L + C_r \frac{dv_c}{dt} = I_d \tag{10}$$

and

$$v_c = L_r \frac{di_L}{dt} \tag{11}$$

When $t \geq t_0$, the equations is represented by (12) and (13)

$$i_L(t) = I_d + (I_{L0} - I_d)\cos\omega_0(t - t_0) + \frac{V_{c0}}{Z_o}\sin\omega_0(t - t_0) \tag{12}$$

and

$$v_c(t) = Z_o(I_d - I_{L0})\sin\omega_0(t - t_0) + V_{c0}\cos\omega_0(t - t_0) \tag{13}$$

In these resonant switching circuits, inductor smoothens the current passing through it while the capacitor reduces the ripple content in voltage across it [8]. The combined LC filter therefore reduces the ripple in the output to a lower level. In the circuit, voltage and current do not conduct simultaneously. Thus, switching takes place only when voltage or current is zero. This type of switching is called soft switching. The chief advantage of the resonant converters is reduced switching loss. Because turn-on or turn-off transitions of the switches occur at zero crossing of the voltage waveform, it reduces or eliminates some of the switching loss [9]. Therefore, resonant converters can operate at higher switching frequencies. Zero voltage switching (ZVS) also reduces the switching stress and converter-generated electromagnetic interference (EMI), consequently reducing the switching power losses.

2.7 Power Losses

The power losses in the SBC circuit can be calculated at switches S_1 and S_2. The top of Figure 12 shows the voltage across the MOSFET and current through it and the bottom shows V_{GS} at the switch as a function of time.

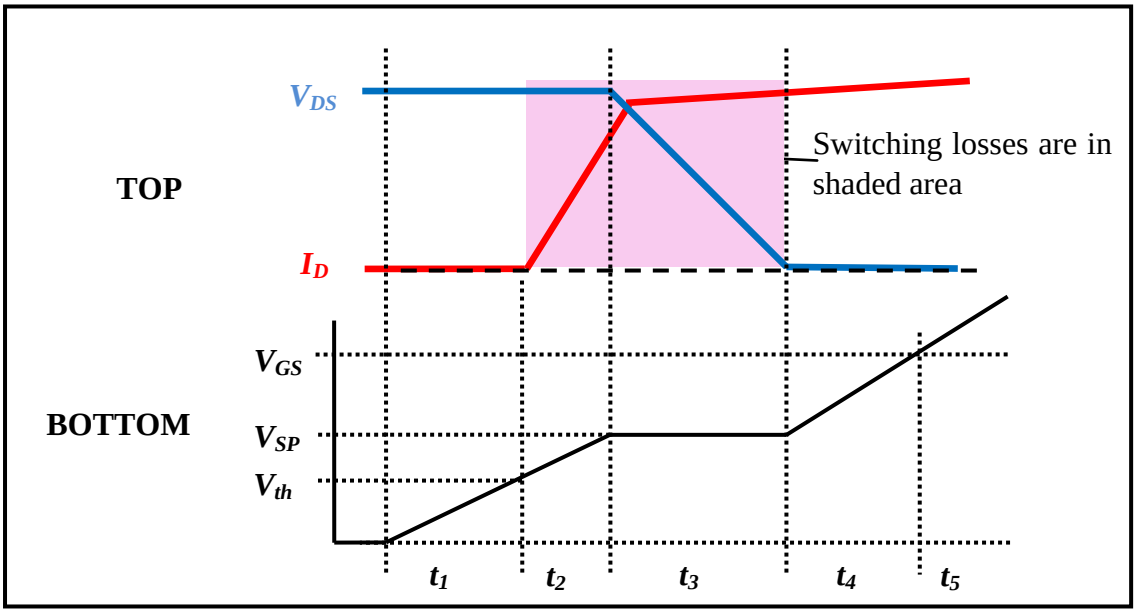


Figure 12 Voltage and current across MOSFET and V_{GS} as a function of time

Switching losses do not occur until V_{GS} reaches its MOSFET's threshold voltage, V_{TH}. Therefore, at power at t_1, P_{t1}=0. At t_2, when V_{GS} reaches V_{TH}, the input capacitance is being charged while the MOSFET's drain current, I_D starts to rise linearly. Referring to Figure 12, the energy in the MOSFET, E_{t2} [7] during t_2 would be represented by (14)

$$E_{t2} = t_2\left(\frac{V_{in} \bullet I_o}{2}\right) \tag{14}$$

where V_{in} = input voltage

I_o = output current at the load, R_{o_load}

Next, in t_3, V_{ds} begins to decrease. t_3 could be though as "Miller time" [7] and the energy at t_3 is interpreted by (15)

$$E_{t3} = t_3\left(\frac{V_{in} \bullet I_o}{2}\right) \tag{15}$$

During t_4 and t_5, the power losses are very small compared to at t_2 and t_3, when the MOSFET is simultaneously sustaining voltage and conducting current. Therefore, it is assumed to be zero in the analysis [7].

Thus, the switching loss for any given edge is the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval represented by (16)

$$P_{SW} = \left(\frac{V_{in} \bullet I_o}{2}\right)(t_2 + t_3)(f_s) \tag{16}$$

where f_s is the switching frequency

In general, the switching power loss at S_1 and S_2 can be represented by (17)

Switching loss, $P_{SW} = P_{t(on)} + P_{t(off)}$

$$P_{SW} = \frac{\left[V_{DS(\max)}\left(I_{DS(on)} \bullet t_{t(on)} + I_{DS(off)} \bullet t_{t(off)}\right) \bullet f_s\right]}{2}$$

$$P_{SW} = 0.5 * \text{switching time} * \text{peak power} * f_s \tag{17}$$

Therefore, total switching loss of both switching would be the addition of $P_{SW,S1}$ and $P_{SW,S2}$ as represented by (18)

$$P_{sw,total} = P_{SW,S1} + P_{SW,S2} \tag{18}$$

Besides switching power loss, conduction loss, P_{cond} and body diode loss, P_{bd} also plays a role in the total power loss, P_{loss_total}. P_{cond} is defined by (19)

$$P_{cond} = (I_{out})^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{out}}{V_{source}}\right) \tag{19}$$

$R_{DS(ON)}$ is a constant and is defined from the datasheet as 0.073Ω.

P_{bd} on the other hand is represented by (20)

$$P_{bd} = 2 \times V_f \times I_{out} \times f_s \times t_{bd} \tag{20}$$

From datasheet, V_f =1.6V.

Therefore, the total power loss, P_{loss_total} is defined by (21)

$$P_{loss,\,total} = P_{cond} + P_{bd} + P_{sw,total} \tag{21}$$

Efficiency of the overall circuit is the ratio of output power, P_{out} to the input power, P_{in} represented by (22)

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{22}$$

To evaluate the percentage of the energy that is actually returned to the power source, an additional parameter energy recovery efficiency, η_{REC} can be defined as

$$\eta_{REC} = 1 - \frac{P_{Loss,V_F}}{P - P_{Loss,R_G}} = \frac{V_{DD}}{V_{DD} + (V_{F1} + V_{F2})} \tag{23}$$

If η_{REC}=90%, it means 90% of the magnetic energy is actually recovered by the power source with the rest 10% wasted on the diodes.

CHAPTER 3
METHODOLOGY

3.1 Procedure

The procedures are carried out and implemented in the project to ensure completion within the given timeframe.

3.1.1 Data research and gathering

Elements of projects involved in this stage include the study of converter circuit, RGD circuit, SBC circuit, MOSFET characteristics, dead time, duty ratio and PSpice simulation. The Gantt chart for the planning of this project is attached in Appendix A.

3.1.2 Project Planning

Figure below shows the flow chart to achieve the objective of this work.

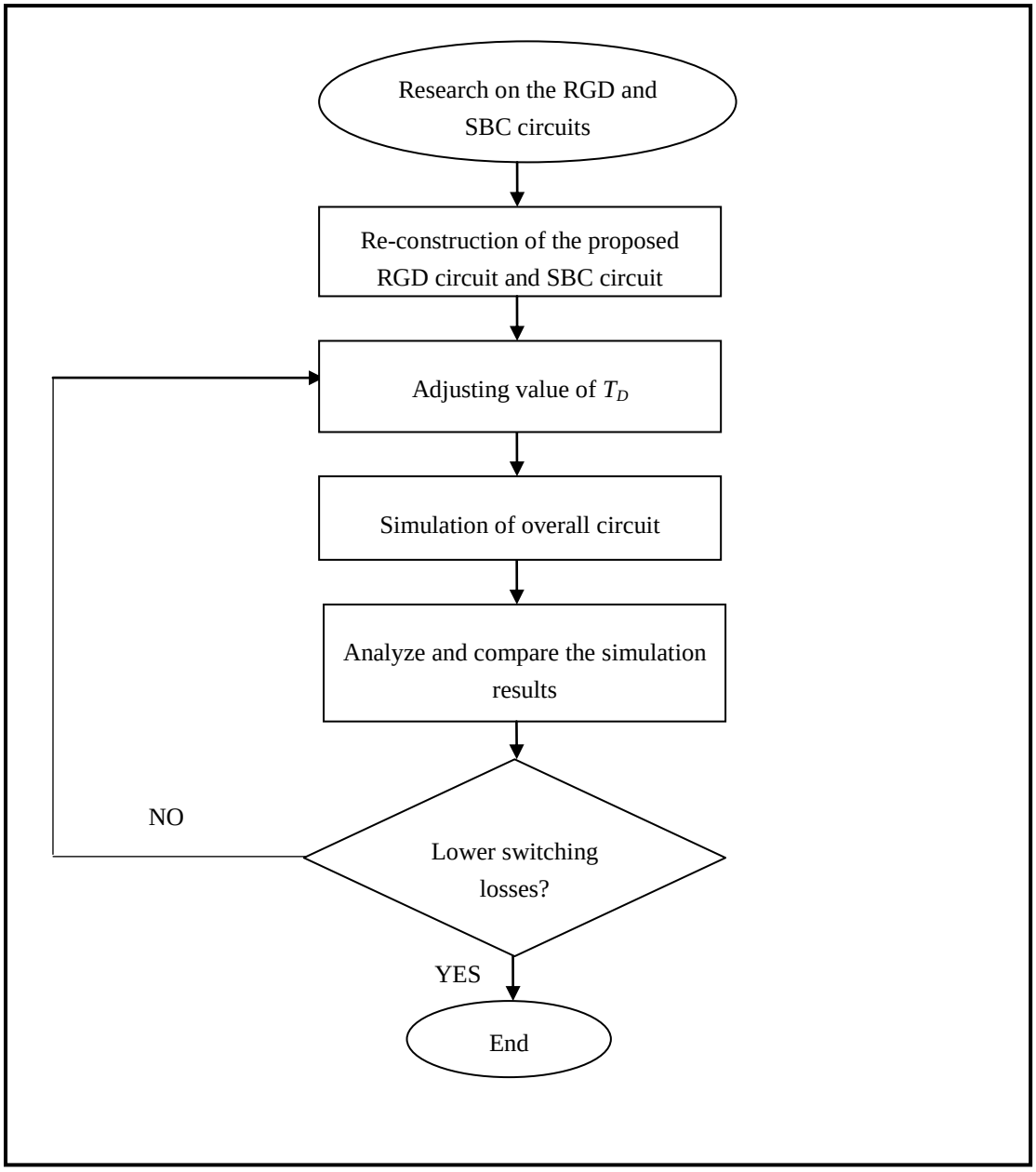


Figure 13 Flow chart of the methodology used in this work

3.1.3 Construct the circuit using PSpice

Firstly, the proposed RGD circuit shown in Figure 6 and the proposed SBC circuit shown in Figure 8 are drawn using Pspice Schematics program. Figure 14 shows the schematics window of the PSpice program.

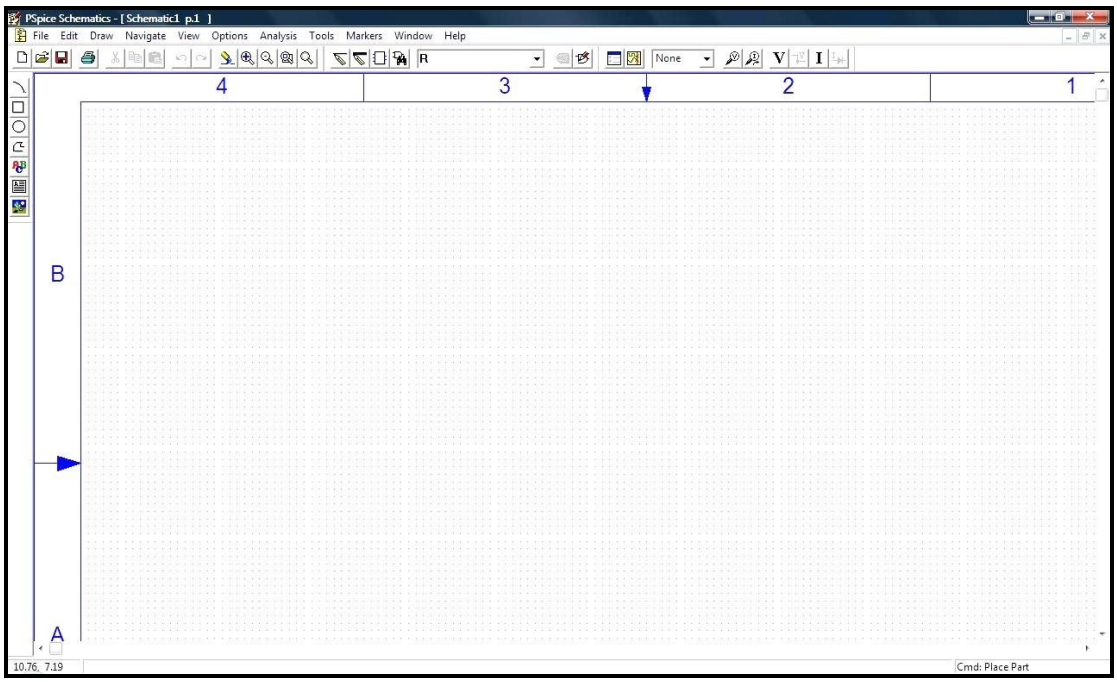


Figure 14 Schematics window of PSpice

To construct the circuit,

- Use ‘Draw’ function to place respective components on schematic
- Click on ‘Get New Part’ as shown in Figure 15
- An alternative or shortcut is by using the keys ‘Ctrl+G’.

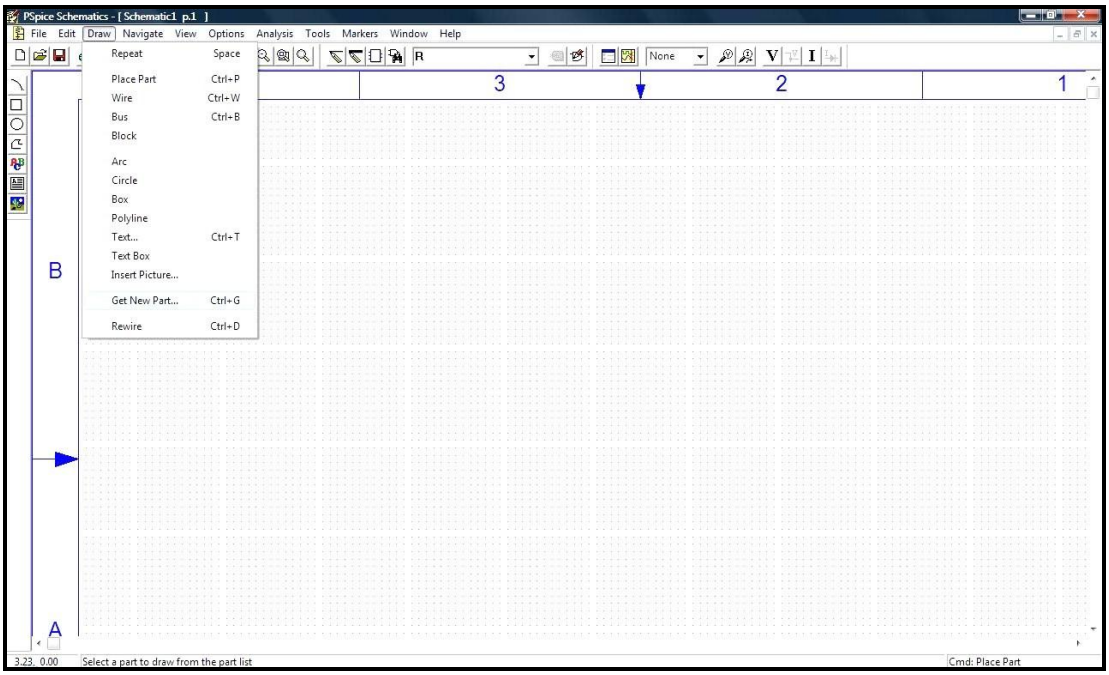


Figure 15 Using 'Draw' function

- A new window for 'Part Browser Advanced' pops-up as shown in Figure 16. This window allows the finding of any parts available in the library of PSpice to be placed on the schematics file.

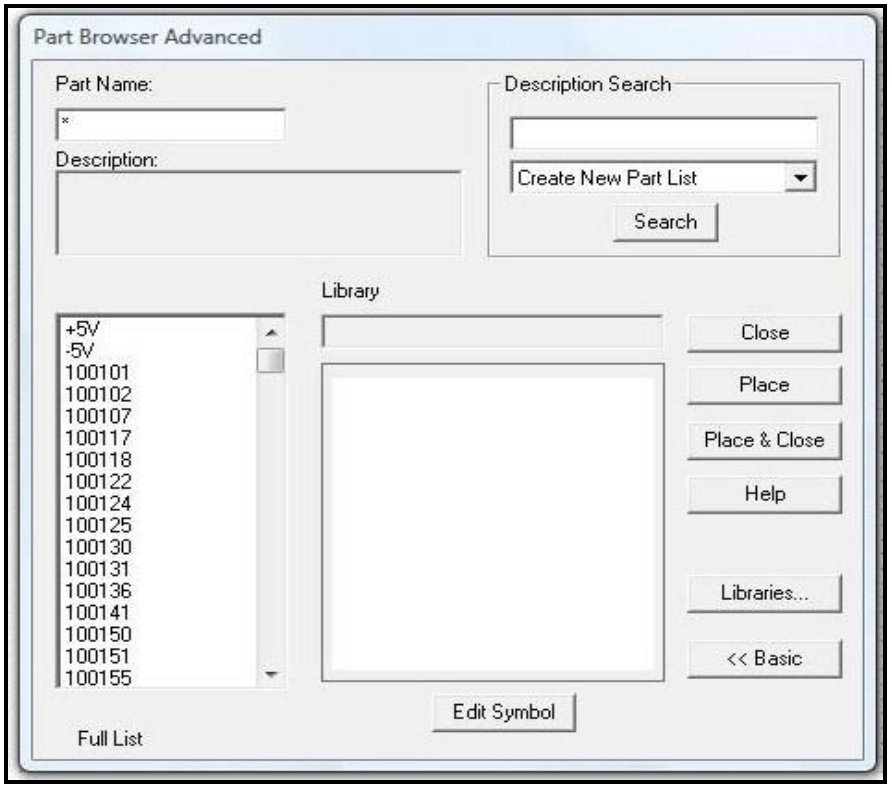


Figure 16 'Part Browser Advanced' window

- Type the name of the component in the space of ‘Part Name’. For example, part name IRFP250 for the circuit is searched as shown in Figure 17.
- Click on ‘Place & Close’ button
- The component is ready to be placed on the schematic diagram

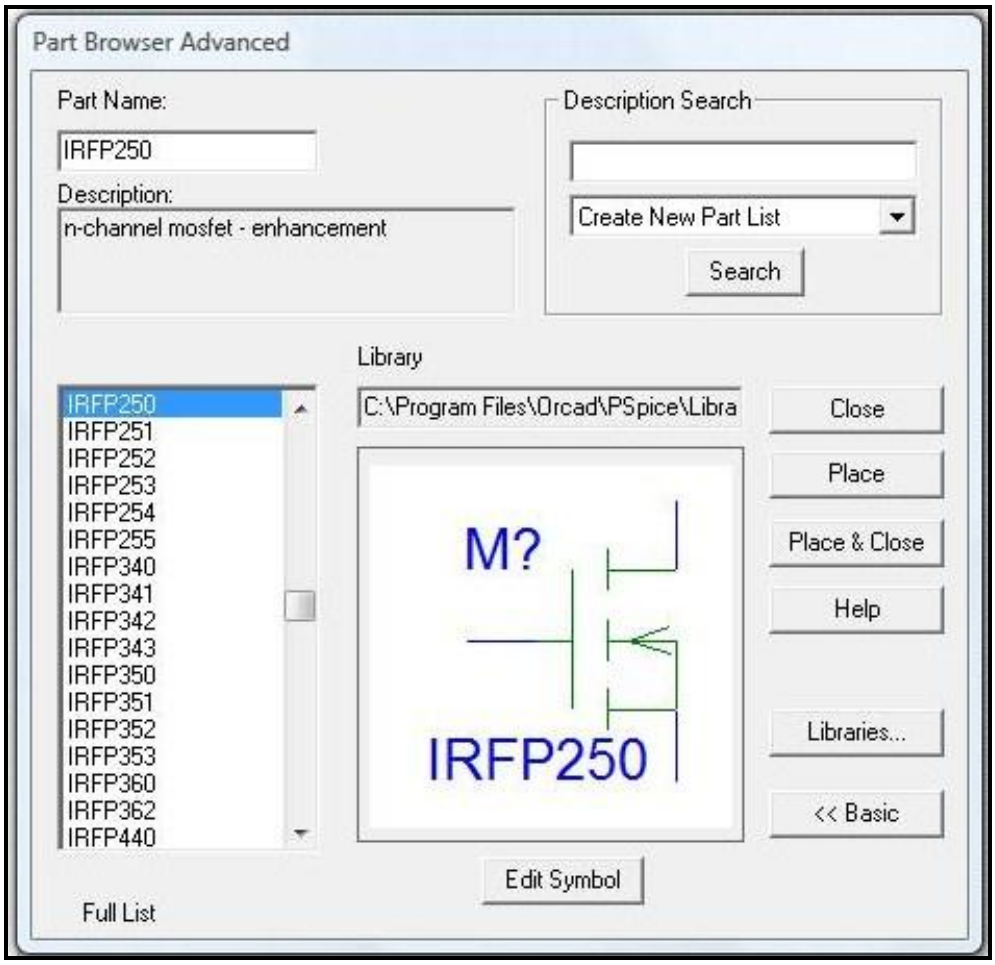


Figure 17 Searching for the component IRFP250

The proposed RGD and SBC circuit is constructed to produce the circuit as shown in Figure 18.

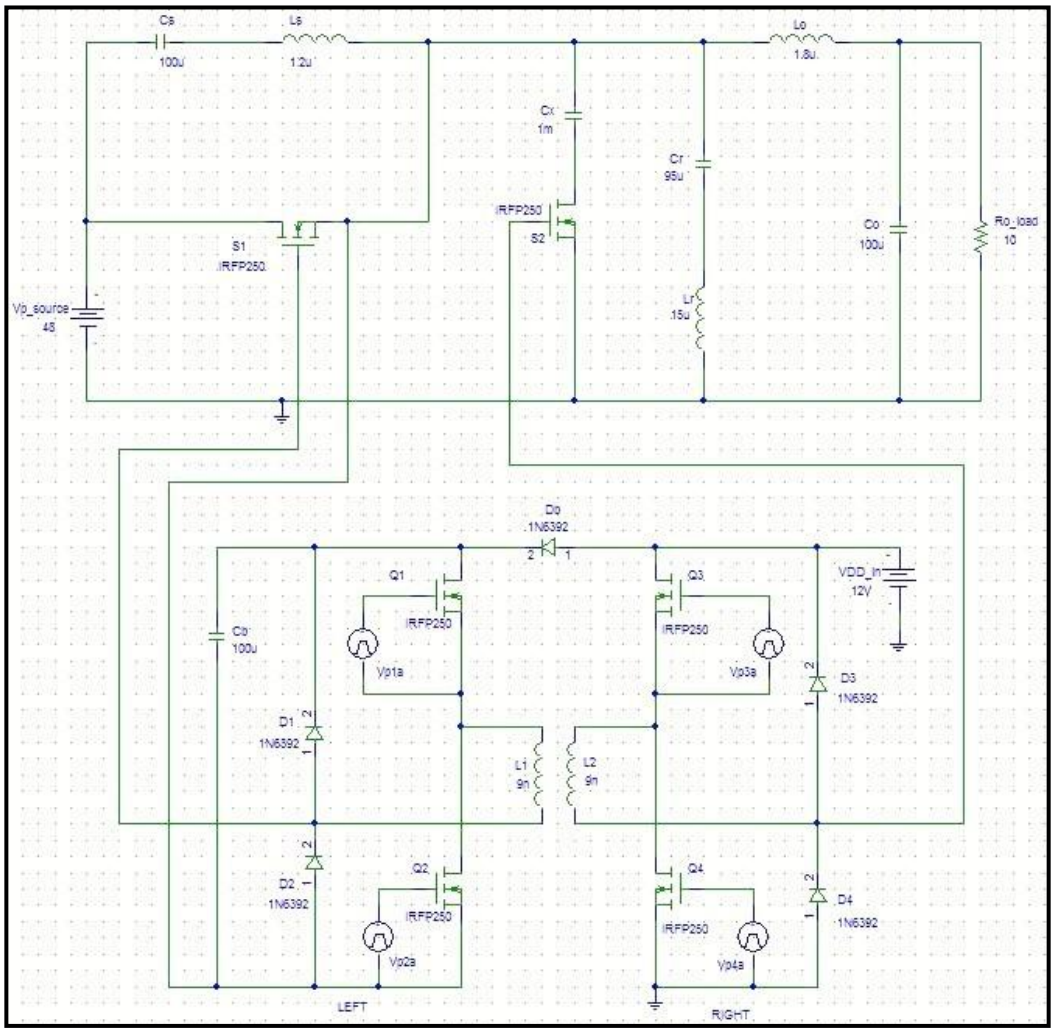


Figure 18 The proposed RGD circuit connected with the proposed SBC circuit

The design parameter for the proposed RGD and SBC follow the same values as in [1]. The values/type of components used in [1] and in this work are tabulated in Table I and II.

Table I Comparing design parameters of proposed RGD circuit in [1] and in this work

Part	**Values/Type**	
	In [1]	**In this study**
V_{DC_in} (V)	12	12
C_b (µF)	100	100
L_1 and L_2 (nH)	9	9
D_1, D_2, D_3, D_4 and D_b	1N6392	1N6392
Q_1, Q_2, Q_3 and Q_4	PSMN130-200D/PLP	IRFP250

Table II Comparing design parameters of proposed SBC circuit in [1] and in this work

Part	**Values**	
	In [1]	**In this study**
V_{p_source} (V)	48	48
L_s (µH)	0.9	0.9
C_s (µF)	100	100
C_x (mF)	1	1
C_r (µF)	95	95
L_r (µH)	15	15
L_o (µH)	1.8	1.8
C_o (µF)	100	100
R_{o_load} (Ω)	10	10
S_1 and S_2	IRFP250	IRFP250

Comparing between [1] and this work, the MOSFET used is different for Q_1, Q_2, Q_3, and Q_4.

3.1.4 Changing the settings for pulse generators

There are 4 different pulses generated for the proposed RGD circuit. Each produces its own pulse of 5 V DC signals. Since the objective of this work is to analyze the dead time, the value of pulse width and dead time of each pulse generator has be modified. To change the settings for *Vp1a*,

- Double click on pulse generator
- The parameter window will appear as shown in the Figure 19
- Click on TD parameter and change it to its desired value
- Click on PW parameter and change it to its desired value
- Click on 'Save Attr' button

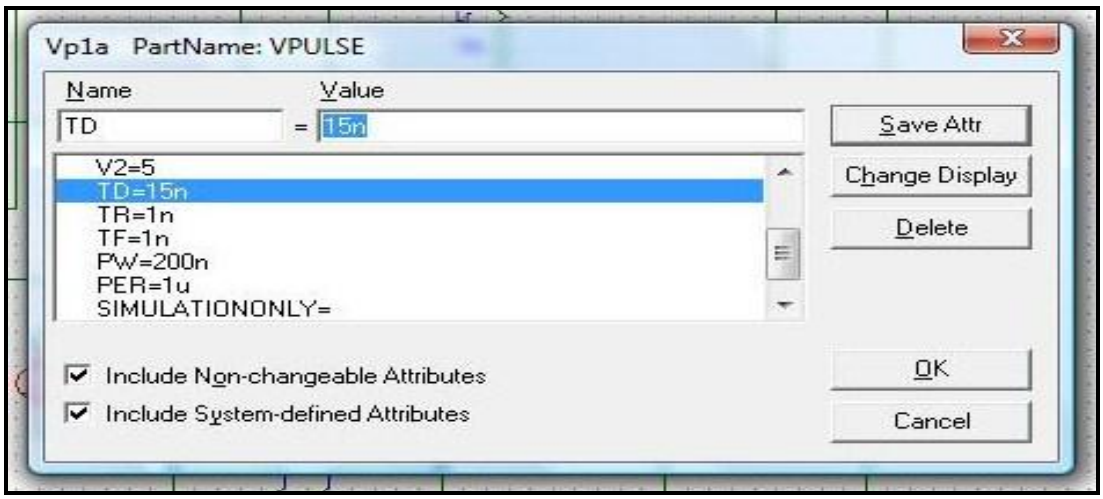


Figure 19 Parameter window for settings of pulse generator 1, *Vp1a*

For example, *Vp1a* settings are listed as follows.

Min Voltage, V_1 = 0 V

Max Voltage, V_2 = 5 V

Time Delay, T_D = 15 ns

Rise Time, T_R = 1 ns

Fall Time, T_F = 1 ns

Pulse Width, PW = 200 ns

Time Taken for a Complete Cycle, PER = 1 μs

The settings of T_D and PW of each pulse generator determines the dead time when both pulses are not conducting. Therefore, T_D and PW for *Vp1a*, *Vp2a*, *Vp3a* and *Vp4a* are adjusted accordingly to obtain varying dead time as shown in Table III. Meanwhile, the inductor values of L_1 and L_2 are set to 9 nH which have been determined in [6] as optimized values.

3.1.5 Obtain operating waveforms of the circuit using PSpice

After the circuit has been constructed and the setup has been completed, the schematic is saved in the designated folder. Next, simulation of the circuit is conducted. To simulate the circuit,

- Click ‘Setup Analysis’ button
- Select ‘Transient’ for the setup configuration.
- Plug-in values of 0 ns for ‘Print Step’ and 3 ms for ‘Final Time’ as shown in Figure 20. The simulation is set up to trace the output for duration of 3000 μs because it is only after 2000 μs that the circuit has reached steady-state as observed in the waveform.

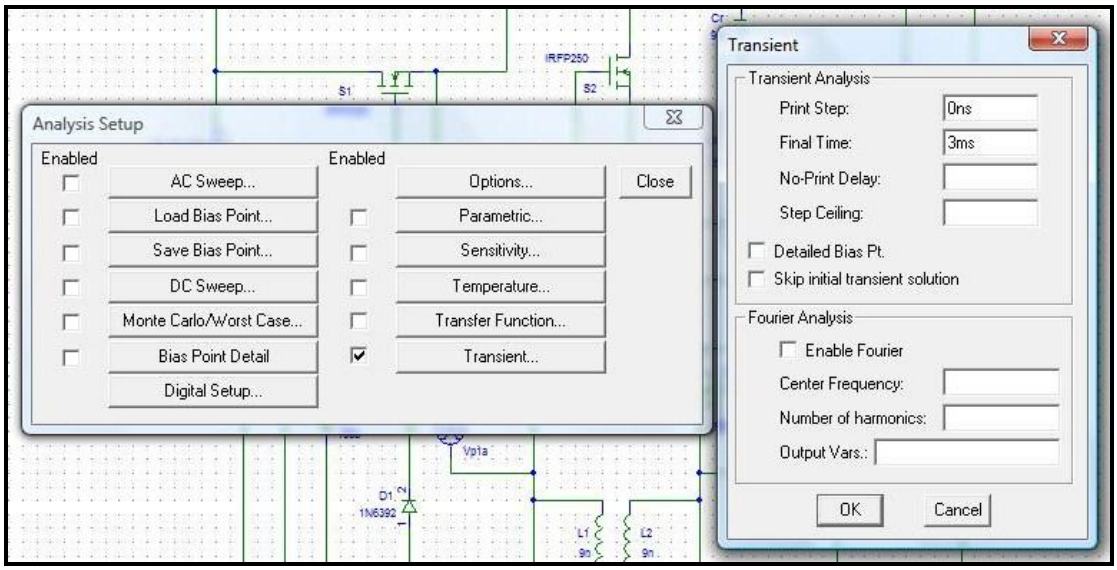


Figure 20 Setup analysis window for transient analysis

The operating waveforms of the proposed RGD circuit can be traced by locating voltage or current markers at the node of the components. To trace the waveforms,

- Select the ‘Marker’ function as shown in Figure 21.

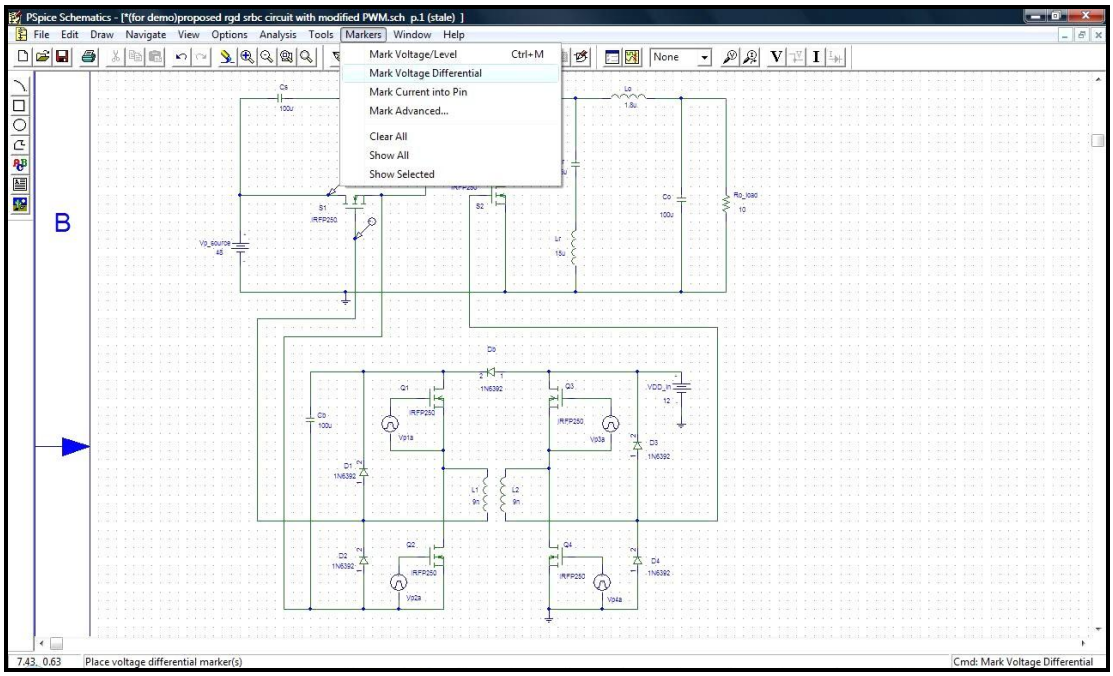


Figure 21 Using the ‘Marker’ function

- Place the ‘+’ and ‘-’ marker on the nodes that analysis has to be done. As an example, the tracing of S_2 gate-source voltage, $V_{gs,S2}$ is shown in Figure 22.

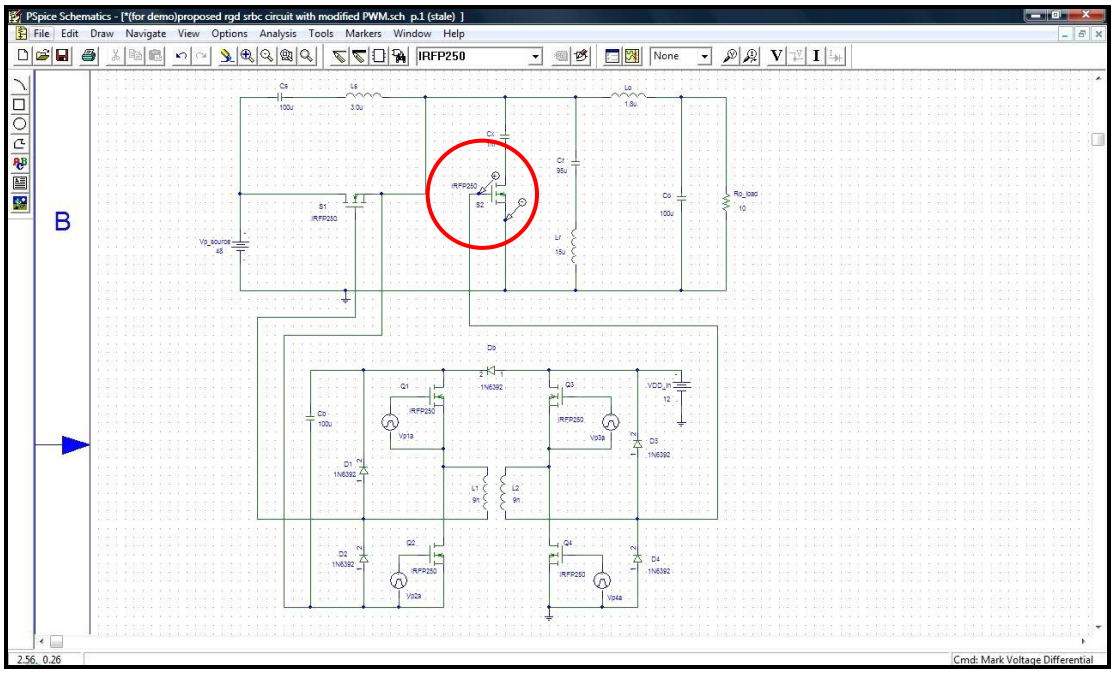


Figure 22 Tracing $V_{gs,S2}$ using the voltage differential marker

- Simulate circuit by using 'Analysis' function and then click on 'Simulate' as shown in Figure 23.
- An alternative way is by pressing the 'F11' key on the keyboard.

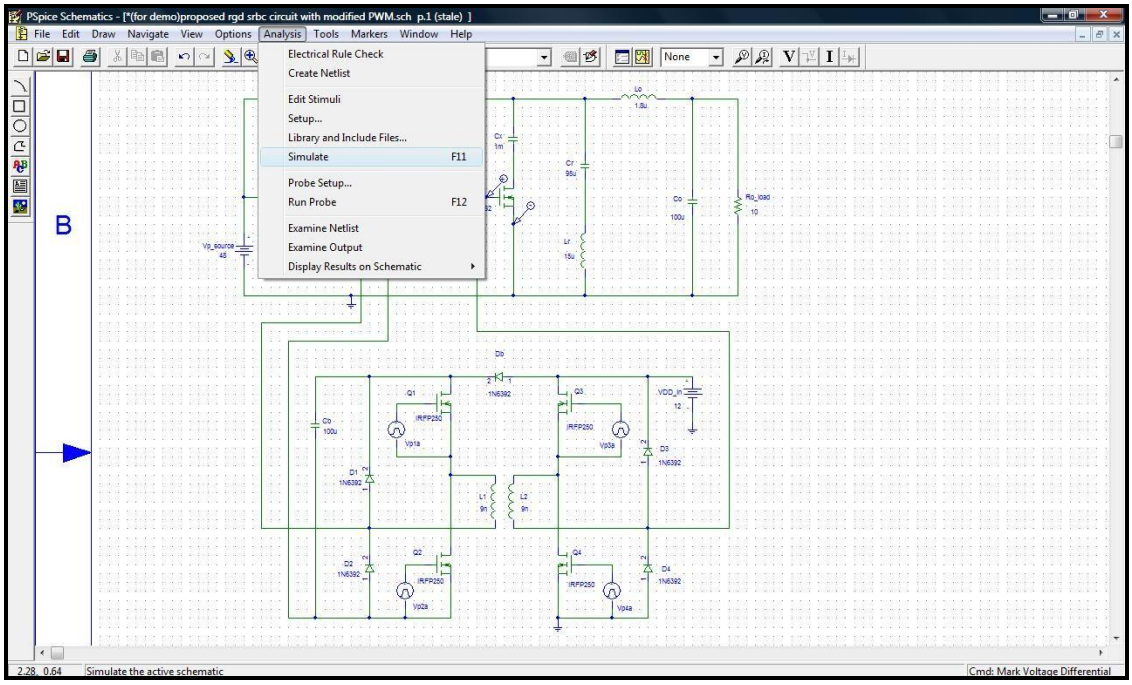


Figure 23 Using the 'Simulate' function

- $V_{gs,S2}$ waveform can be viewed in the PSpice A/D window for further analysis

3.1.6 Finding switching losses in the circuit

To find the switching losses,

- Use ‘Trace’ and ‘Add Traces’ application in the PSpice A/D window as shown in Figure 24.
- For shortcut, the ‘Insert’ key can also be used.

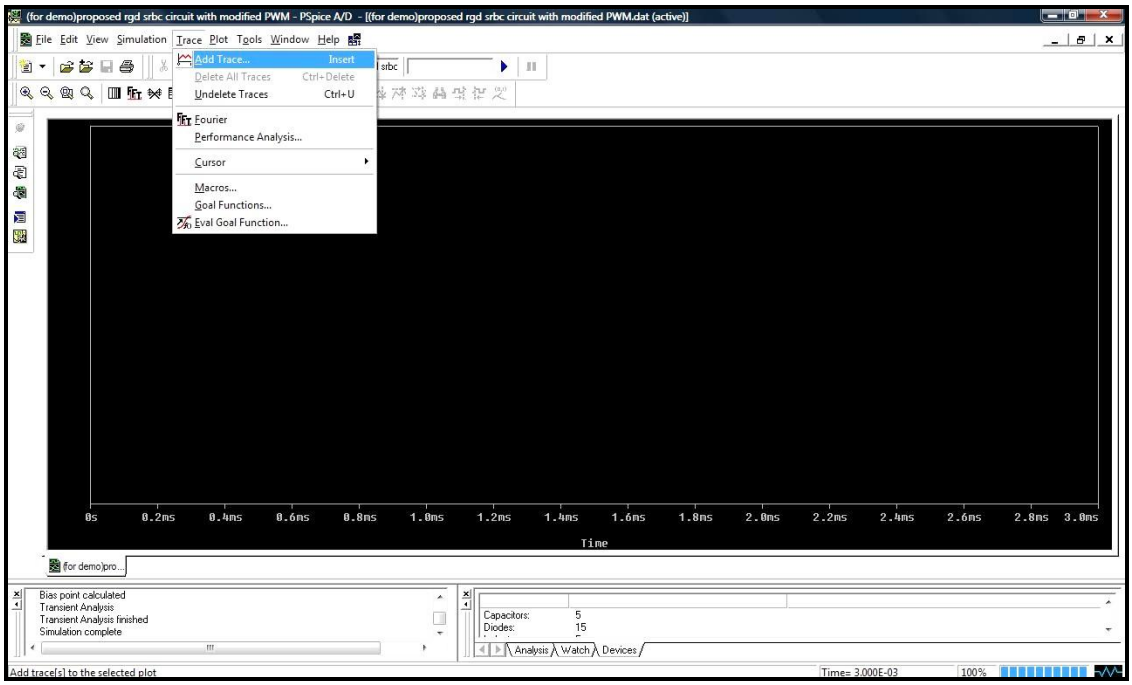


Figure 24 ‘Add trace’ function

In this work, switching losses is demonstrated by the peak power at both S_1 and S_2. To obtain the turn-off and turn-on peak waveforms of both switches, the peak power formula is included by,

- Writing the S_1 turn-off peak power formula ($V_{ds,S1}$*$I_{d,S1}$) in the trace expression space provided as shown in Figure 25.
- The same function is used to generate the S_2 turn-on peak($V_{ds,S2}$*$I_{d,S2}$).

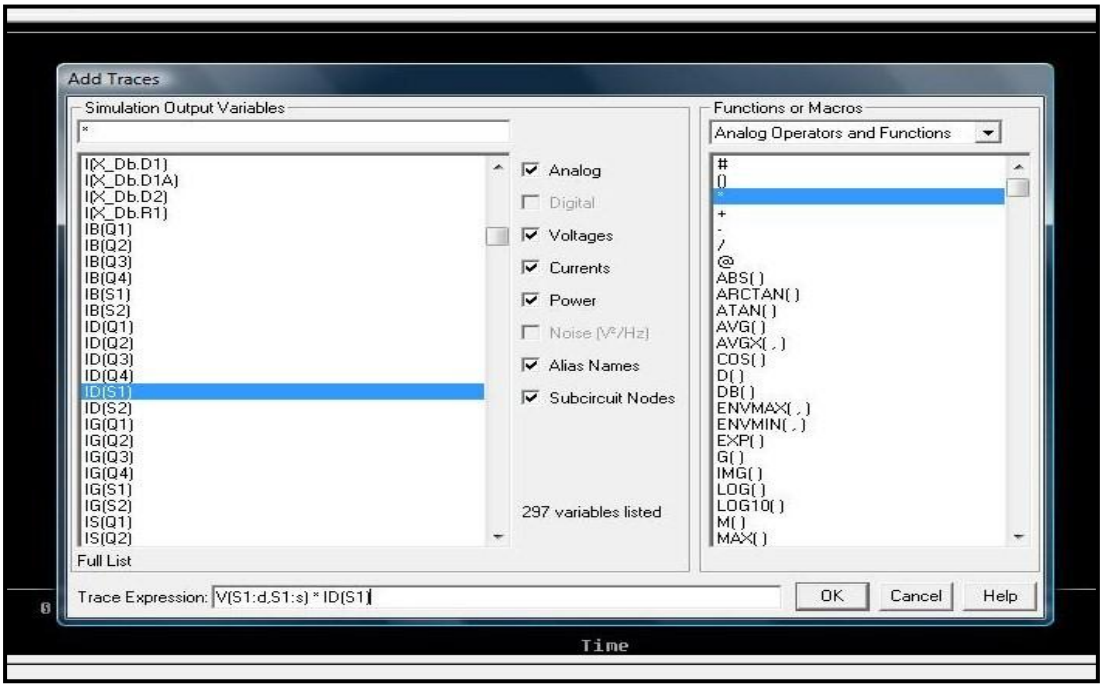


Figure 25 "Add traces" application window

The operating waveforms can be further analyzed by zooming in so that a clearer waveform can be seen. This is done by,

- Using the 'Plot' function and adjusting the 'Axis Settings' values as shown in Figure 26.

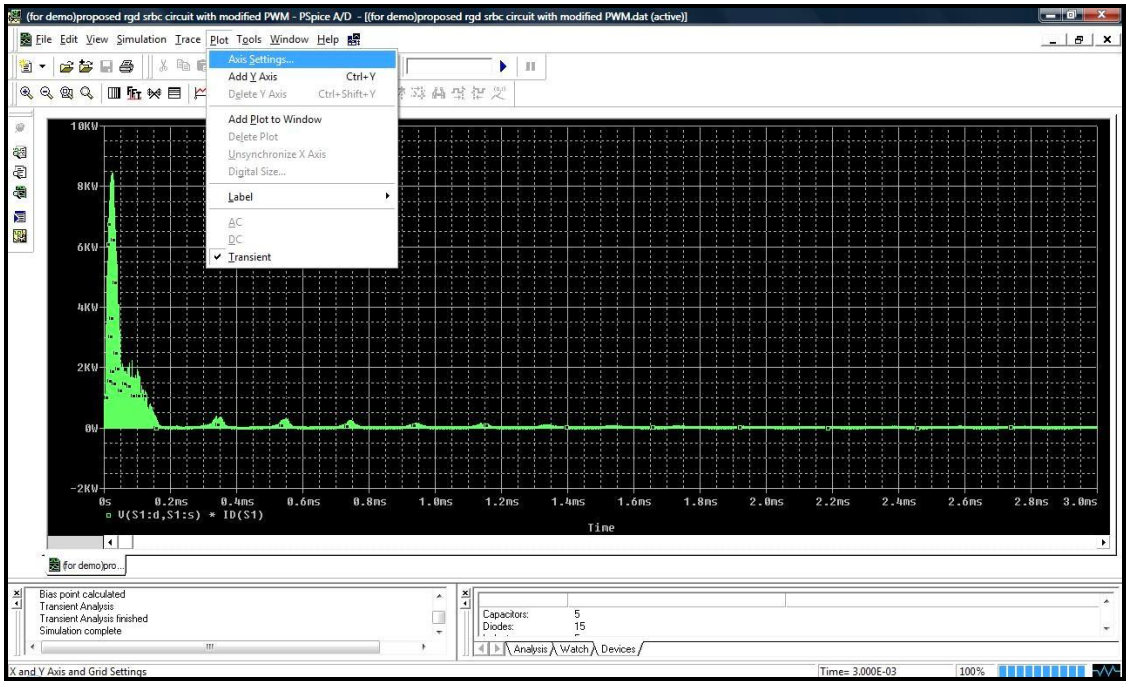


Figure 26 Using the 'Axis Settings' function in PSpice

- In ‘Axis Setting’, x-axis, y-axis, x-grid and y-grid can be adjusted as desired. For example, the operating waveform of turn-off switching loss for S_1 is set from 1.2388 ms to 1.2397 ms as shown in Figure 27.

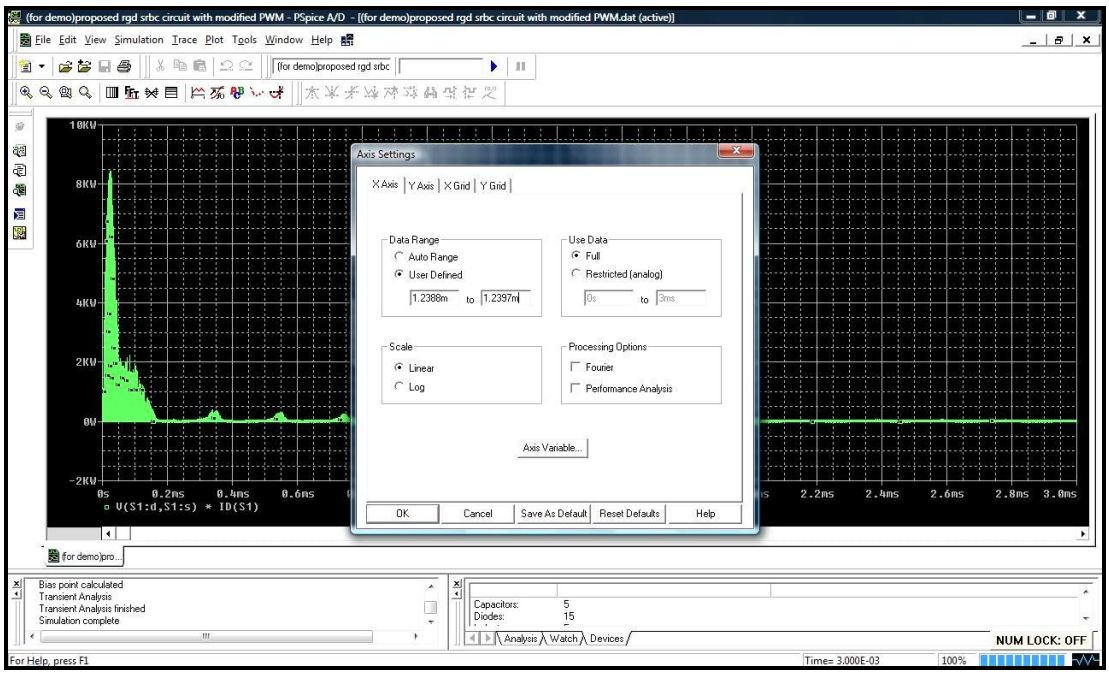


Figure 27 X-axis setting for turn-off switching loss for S_1

This results in a more comprehensible operating waveform that is easier to be analyzed as shown in Figure 28.

Figure 28 A more comprehensible graph obtained using PSpice

3.1.7 Analyzing operating waveforms in PSpice

PSpice offers various functions to analyze the graphs generated.

- The highest and lowest peak of a graph can be identified using the 'Toggle cursor' button at the toolbar as shown in Figure 29.

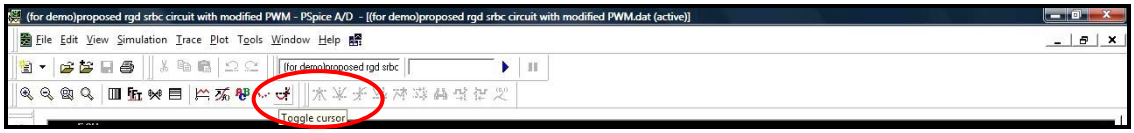


Figure 29 'Toggle cursor' button application

- The 'Probe Cursor' is activated for analysis purposes as shown in Figure 30, for example, identifying the peak positive and negative value of the graph.
- 'Probe Cursor' provides the x-axis and y-axis values of the graph obtained

Figure 30 'Probe Cursor' application in PSpice

After obtaining the values from the graphs generated, analysis of the results is carried out. Most results are tabulated and line graphs are drawn using Microsoft Excel for a better understanding of the results. Details on the analysis are also discussed.

3.1.8 Generating graphs using Mathcad program

The primary window of the Mathcad program is shown in Figure 31.

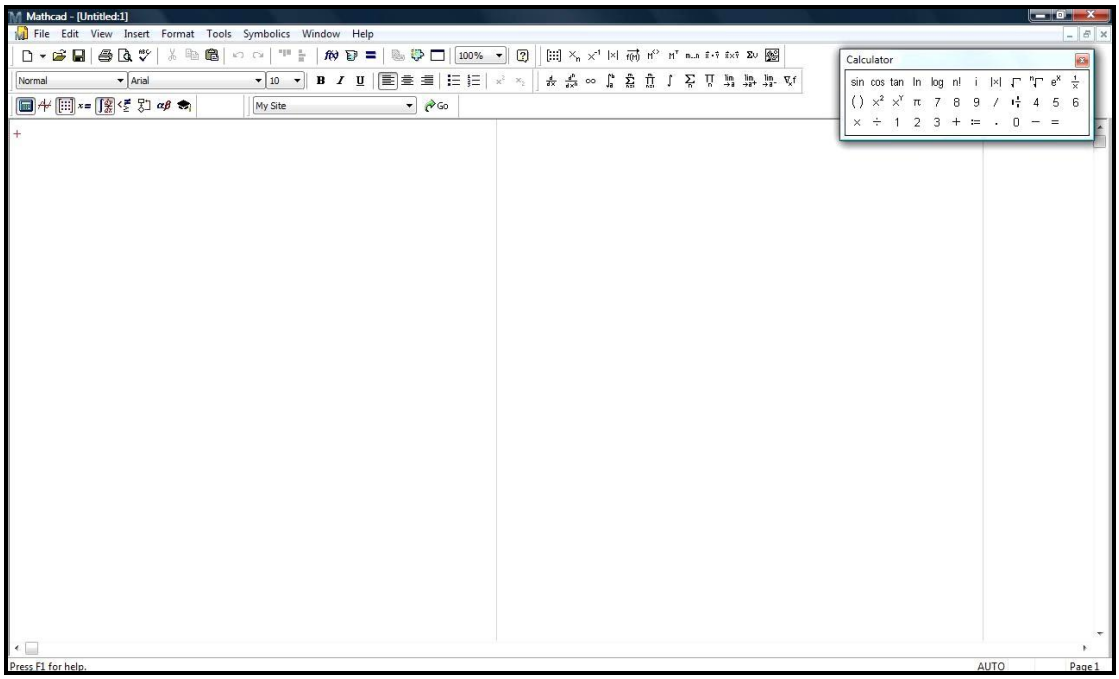


Figure 31 Primary window of Mathcad

Before using the Mathcad program, the formulas for the graph are identified first. To obtain graphs from Mathcad,

- Constant values are defined as shown in Figure 32. All constant values must be defined first before formulas are included, or else Mathcad would not be able to identify and calculate the final values.

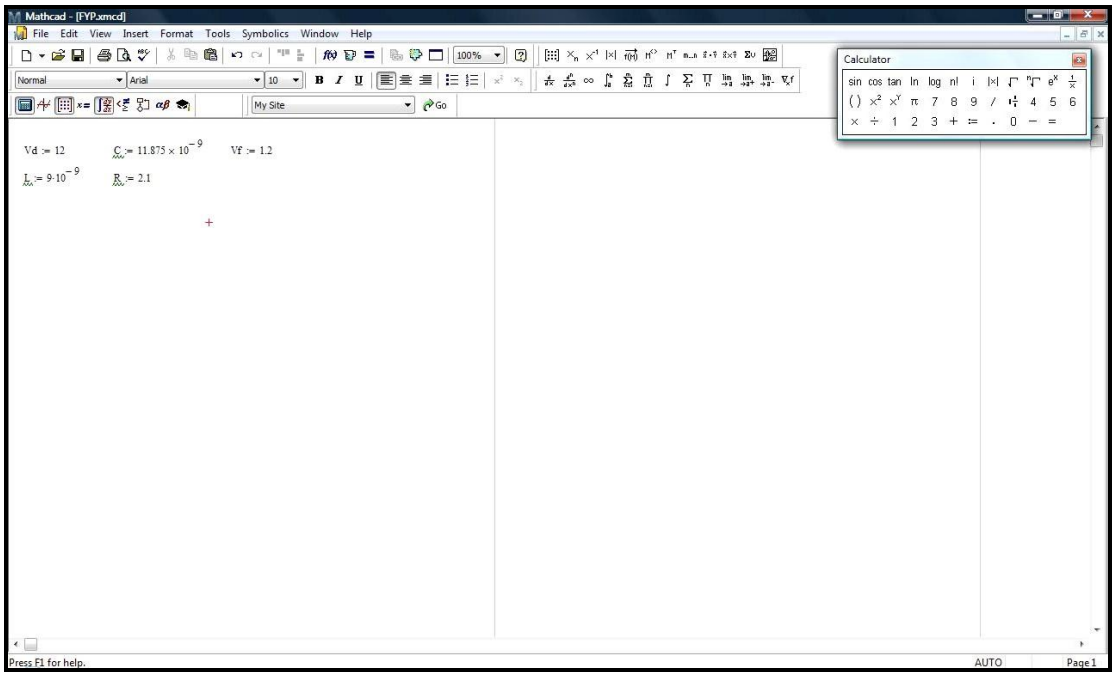


Figure 32 Defining constant value in Mathcad

- Insert formulas. For example, the formula for i_{L1} is shown in Figure 33.

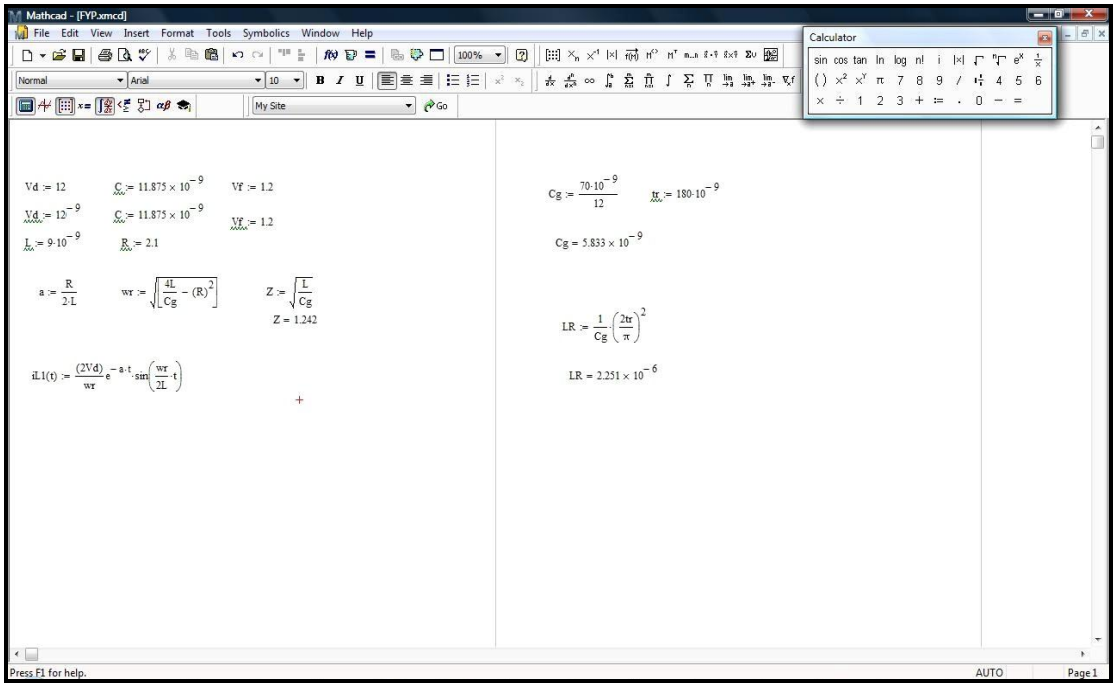


Figure 33 Insert i_{L1} formula in Mathcad

- Generate the graph by using the function ‘Insert’ and ‘Graph’.
- Click on ‘X-Y Plot’ to obtain the graphs desired as shown in Figure 34.

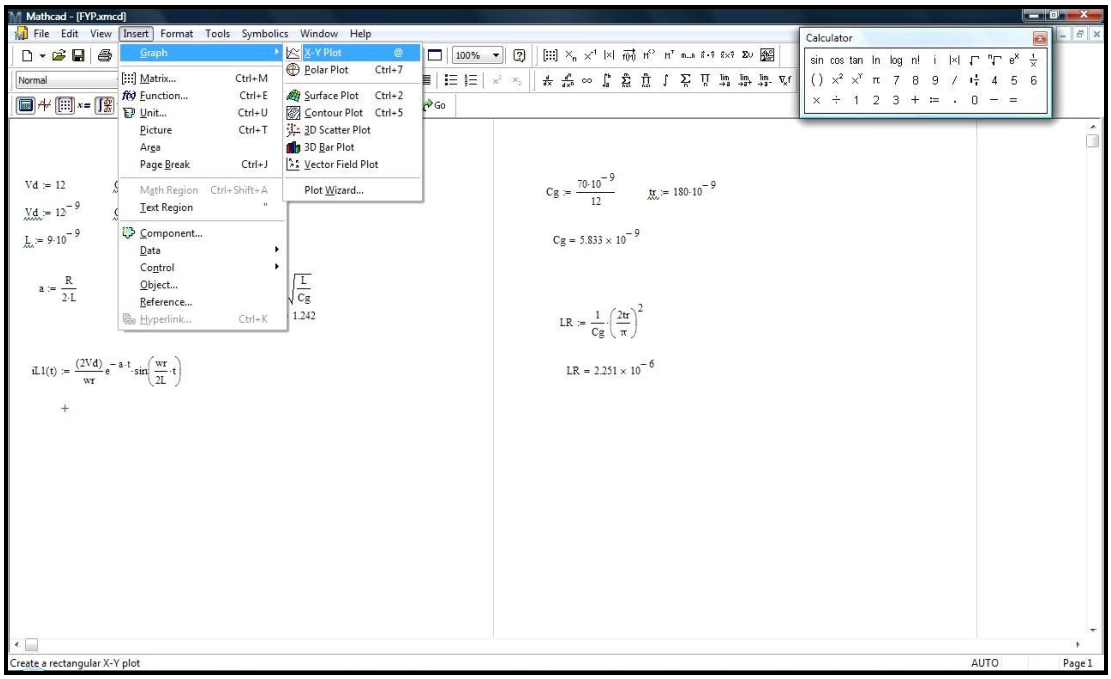


Figure 34 Using the ‘X-Y Plot’ function in Mathcad

- An X-Y graph appears
- The beginning and end values of the x-axis as well as the function at y-axis need to be filled so that the graph can be generated. An example is the i_{L1} graph generated as shown in Figure 35.

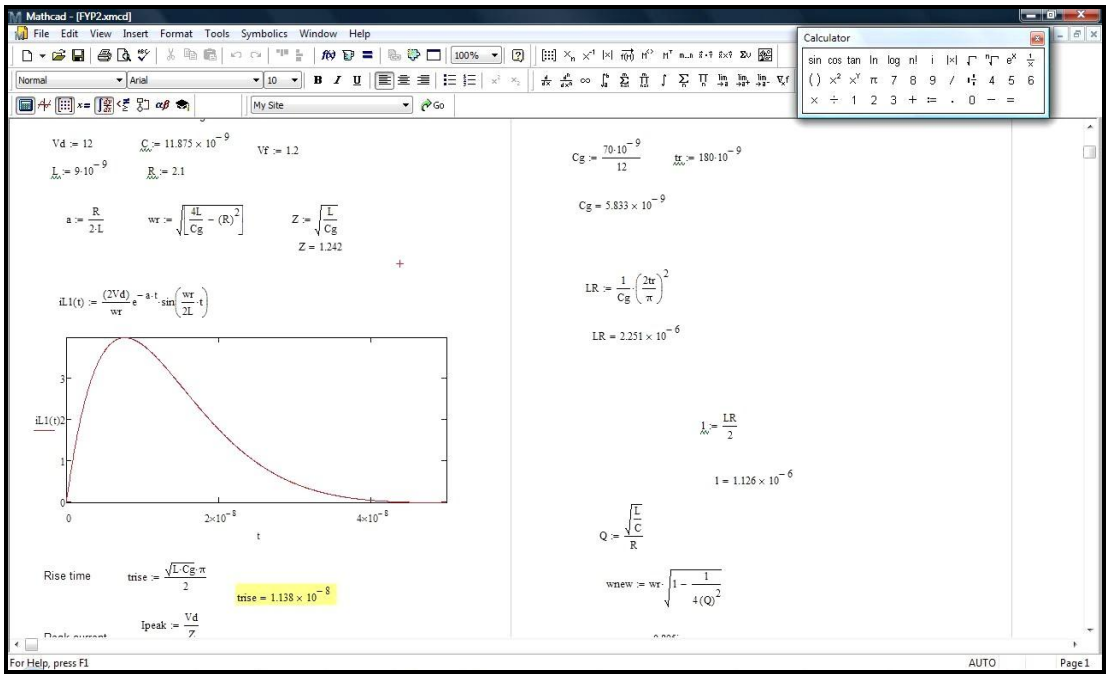


Figure 35 i_{L1} graph generated using Mathcad

From the graph generated, analysis can be done. The gradient of the graphs are calculated manually and compared to the graph generated in PSpice.

3.1.9 Analyzing graphs in Mathcad

After the generated graphs are obtained, analysis of the graphs in Mathcad is done manually. Calculation of gradient of the slope is computed by following the formula represented by (24)

$$Gradient, m = \frac{y_1 - y_2}{x_1 - x_2} \tag{24}$$

Following that, these current and voltage values are compared with the values obtained from PSpice and the difference is calculated.

After all the simulations have been done, analysis of the results is carried out. Most results are tabulated and line graphs are drawn using Microsoft Excel for a better understanding of the results. Details on the analysis are also discussed in every section.

3.2 Tools

The programming tools needed for this work are PSpice Schematics Version 9.2 Copyright® 1986-2000 by Cadence Design Systems, Inc. and Mathcad Version 14.0 Copyright © 2007 by Parametric Technology Corporation.

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Proposed RGD Circuit

The settings on each pulse generator in the proposed RGD circuit of Figure 6 are shown in table below while Figures 36-38 indicate the readings consist of dead time, delay time and pulse width.

Table III Settings for pulse generators in proposed RGD circuit

Dead time		Initial delay time, $t_{d,\,initial}$ (ns)	Delay time for each voltage pulse				Pulse Width					
T_D= T_{D1}= T_{D2} (ns)	T_{D3} (ns)		t_{d1} (ns)	t_{d2} (ns)	t_{d3} (ns)	t_{d4} (ns)	PW_1 (ns)	PW_2 (ns)	PW_3 (ns)	PW_4 (ns)	PW_{S1} (ns)	PW_{S2} (ns)
5	23	15	15	222	284	947	200	786	654	331	201	661
15	15	15	15	232	284	955	200	765	654	312	211	670
30	5	15	15	247	284	969	200	740	654	286	229	689

The dead time are varied in order to evaluate the performance of the circuit. For different dead times, the initial delay time, $t_{d,initial}$ is set to be constant at 15 ns. Therefore, the first delay time for voltage pulse one, t_{d1} is equal to $t_{d,initial}$. By taking T_D=15 ns as reference, it can be observed that only delay time for voltage pulse 1 and 3, t_{d1} and t_{d3} , and pulse width of voltage pulse of 1 and 3, PW_1 and PW_3, are changed in order to obtain the dead times of 5 ns and 30 ns. The table also shows that when T_{D1}=T_{D2} increases, T_{D3} decreases instead.

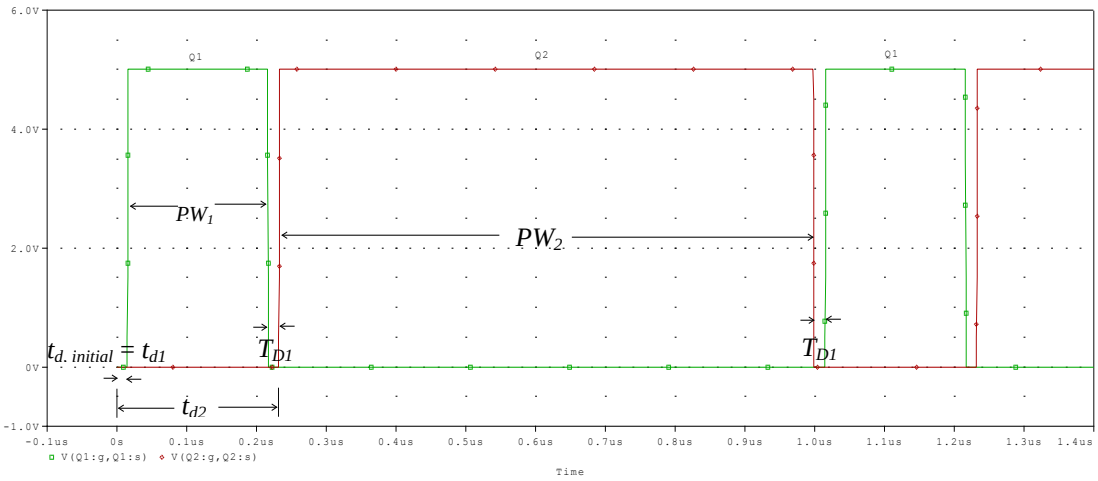


Figure 36 Indication of pulse width, dead time and delay time for Q_1 and Q_2 MOSFETs for T_D=15 ns

The graph of Figure 36 is generated from the simulation of $V_{gs,Q1}$ and $V_{gs,Q2}$. Both Q_1 and Q_2 MOSFETs conduct complementarily of each other. The time in between when both MOSFETs are not conducting is known as the dead time, T_{D1}. PW_1 is the pulse width of Q_1 and similarly is PW_2 the pulse width of Q_2. $t_{d,\ initial}$ which is equal to t_{d1} is the initial delay time, set at a constant value of 15 ns. t_{d2} on the other hand is the delay time before Q_2 starts to conduct.

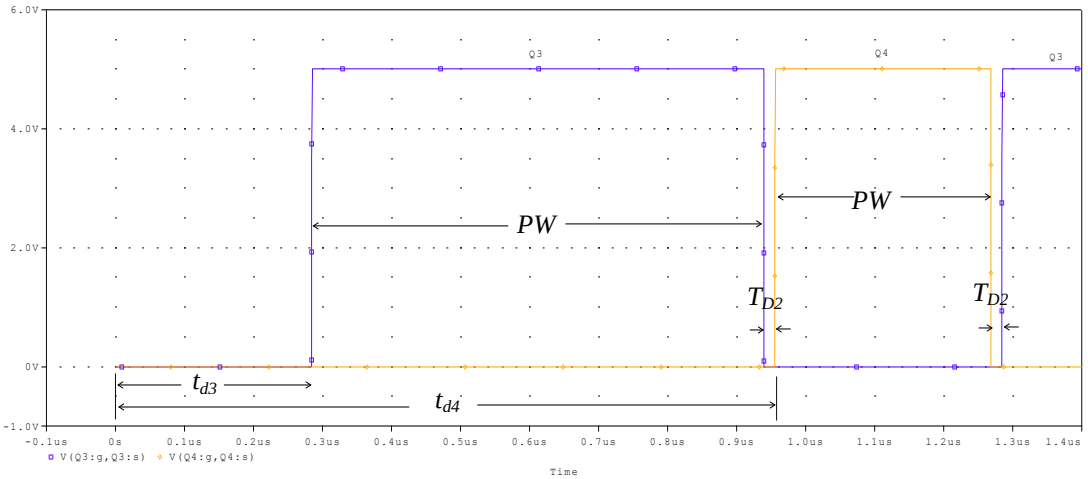


Figure 37 Indication of pulse width, dead time and delay time for Q_3 and Q_4 MOSFETs for T_D=15 ns

Figure 37 shows the indication of pulse width for Q_3, PW_3 and Q_4, PW_4. t_{d3} is the delay time before the MOSFET Q_3 starts to conduct. Similarly, t_{d4} is the delay time before Q_4 starts to conduct. On the other hand, T_{D2} is the dead time when both

MOSFETs, Q_3 and Q_4 are not conducting.

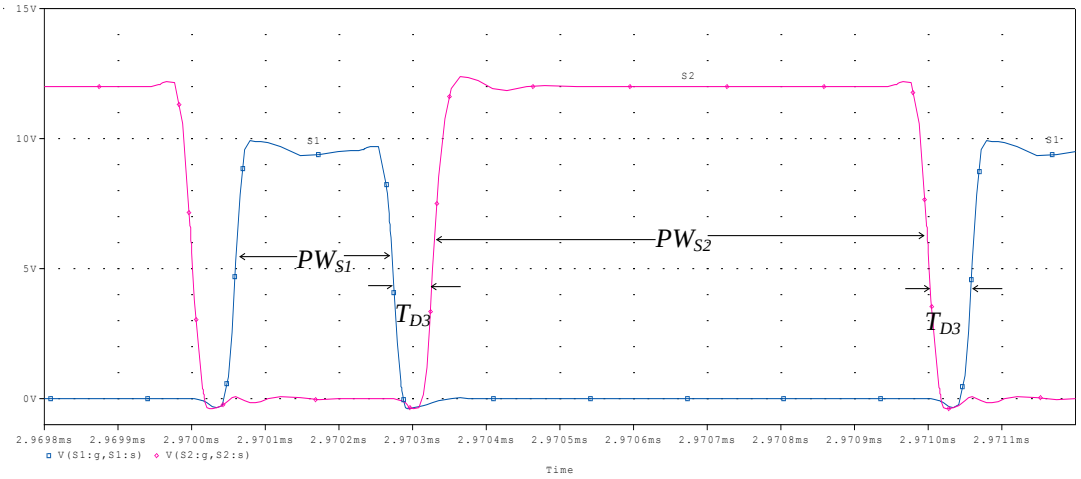


Figure 38 Indication of pulse width and delay time for S_1 and S_2 switches for T_D=15 ns

The graph above is generated for the gate source voltage of both switches, $V_{gs,S1}$ and $V_{gs,S2}$. The maximum of $V_{gs,S1}$ is at 10V and PW_{S1} is the pulse width of S_1. $V_{gs,S2}$ goes to a maximum value of 12 V with pulse width PW_{S2}. T_{D3} is the dead time when both switches are not conducting. The value of $V_{gs,S1}$ should be equal to $V_{gs,S2}$ at 12 V in order to have balanced voltages. But because of the addition of C_x in the proposed SBC circuit, there is a voltage drop of 1.7 V. Therefore, the simulation shows a result of $V_{gs,S1}$ = 12 – 1.7 = 10.3 V $\approx$ 10 V. The purpose of adding C_x to the circuit is to eliminate floating voltages at $V_{gs,S2}$ so that there is less conduction losses in the circuit.

Since both $V_{gs,S1}$ and $V_{gs,S2}$ are not of the same amplitude, the internal capacitance, C_{in} for both switches are not the same. C_{in} can be obtained from the basic formula defined by the equation

$$Q = CV \tag{25}$$

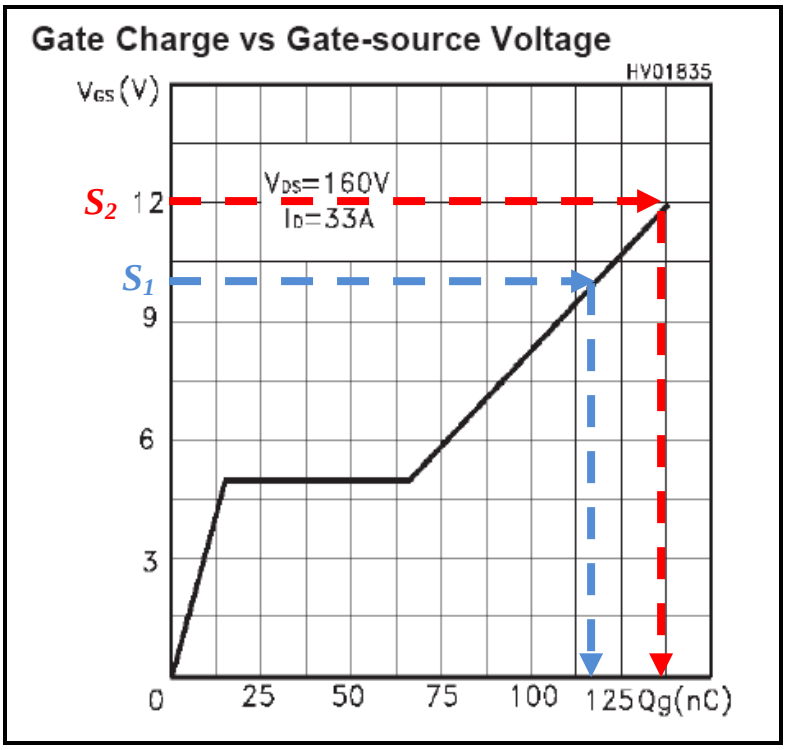


Figure 39 Gate charge versus gate-source voltage graph

From the datasheet of IRFP250, the gate charge versus gate-source voltage graph is obtained as shown in Figure 39. For this work, since $V_{gs,\,S1}$ equals to 10 V, C_{in} of S_1 is,

$$C_{in,S1} = \frac{118.75\text{ nC}}{10\text{ V}} = 11.875\text{ nF}$$

On the other hand, $V_{gs,\,S2}$ operates at 12 V, giving the internal capacitance as,

$$C_{in,S2} = \frac{137.5\text{ nC}}{12\text{ V}} = 11.458\text{ nF}$$

The graph below shows the operating waveforms generated from the left hand side of the proposed RGD circuit in Figure 6 after the circuit is simulated. This is shown in Figure 40 below.

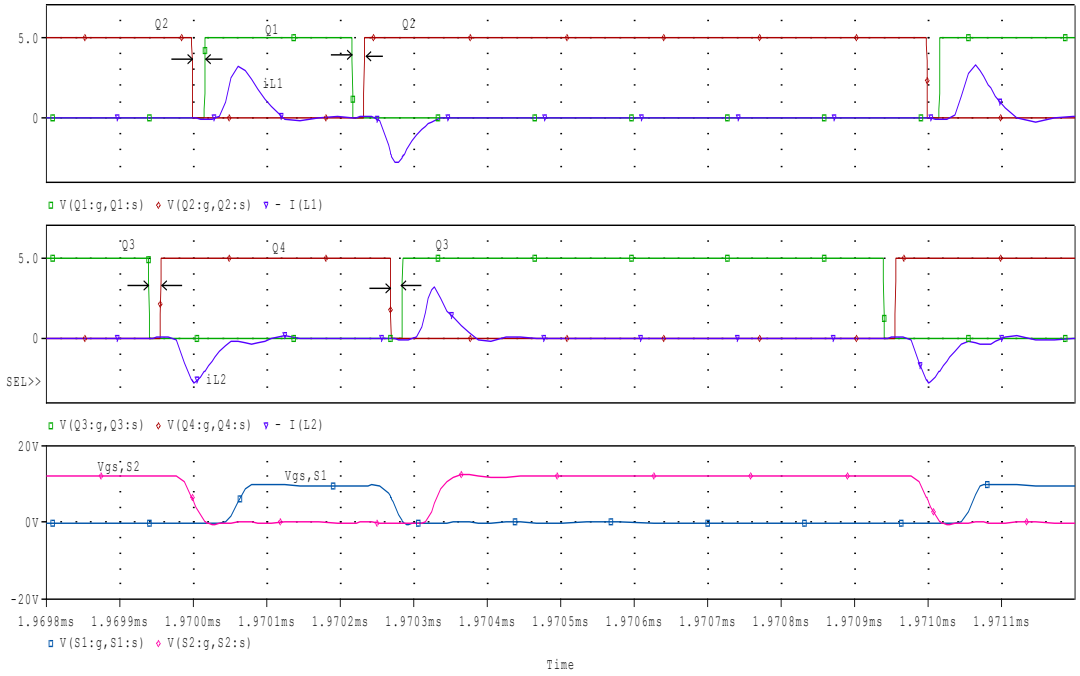


Figure 40 Operating waveforms of the proposed RGD circuit

Pulses from *Vp1a* and *Vp2a* are fed into the MOSFETS, Q_1 and Q_2 on the left hand side of RGD circuit. From the waveform, Q_1 and Q_2 are complementary driving pair inherited from the conventional driver. First, when Q_1 is switched on, the inductor current of the left circuit, i_{L1} starts to conduct and it is charged to maximum. The characteristic impedance of the resonant circuit can be represented by (26)

$$Z_o = \sqrt{\frac{L_R}{C_{in}}} \tag{26}$$

where L_R is the resonant inductor equivalent to 9 nH

The rise time t_r can be estimated by (27)

$$t_r = \frac{\pi}{2 \times w_O} = \frac{\pi}{2} \times \sqrt{L_R \bullet C_{in}} \tag{27}$$

where w_o is the resonant frequency

The duration of this charging current depends on the value of L_R for being the time constant of the circuit. If the duration of the discharging current is not sufficient, it will cause current oscillation when Q_1 is turned off [1]. On the other hand, D_1 and D_2 are designed to clamp V_{gs} and to provide low impedance path for the inductor current and recover the driving energy which is represented by (28)

$$t_{rec} = \pi \sqrt{L_R \bullet C_{in}} \tag{28}$$

where V_{DD_in} is the input voltage

On the other hand, the peak time is defined by (29)

$$t_{rec} = \frac{\tan^{-1}\left(\dfrac{2L_R \times \sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}}{R} \right)}{2 \times \sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}} \tag{29}$$

where R_G is the total gate resistance

After i_{L1} has been fully charged to peak current and at the same moment $V_{gs,S1}$ is clamped at V_{DD_in} by diode D_1, i_{L1} flows according to the path Q_1, L_1 , $V_{gs,S1}$. The inductor current can be represented by equation (30)

$$i_{L1}\left(t_{peak}\right)=\frac{2V_{DD\_in}}{\sqrt{\frac{4L_R}{C_{in}}-{R_G}^2}}\bullet e^{-\frac{R_G}{2L_R}\bullet t}\bullet\sin\left(\frac{\sqrt{\frac{4L_R}{C_{in}}-{R_G}^2}}{2L_R}\bullet t\right) \tag{30}$$

i_{L1} then starts to discharge back to zero through $Q_{2,body\ diode}$, L_1 , D_1 and back to V_{DD_in}, the direct current source at 12 V. After a predetermined T_D of either 5 ns, 10 ns or 15 ns, Q_2 will turn on instead. At this time Q_1 is turned off. Then i_{L1} starts to charge again but to a negative maximum value. This value will be a little lower compared to the positive value of i_{L1} because of leakage current. i_{L1} shows a symmetrical behavior compared to when Q_1 is conducting. When i_{L1} increases back to zero, it goes through D_2, L_1, $Q_{1,body\ diode}$ and to V_{DD_in}. With circuit symmetry between charging and discharging, the total R_G power loss is given by equation (31)

$$P_{loss\_R_G}=2\times\int_{t_1}^{t_2}\left({i_{L1}}^2\bullet R_G\right)\bullet dt\approx\frac{R_G}{\left(R_G+Z_O\right)}\times Q_{DD}\times V_{DD\_in}\times f_s \tag{31}$$

where t_1 is the rise time of the inductor current

t_2 is the recovery time of the inductor current

The same operation goes for the right hand side of the proposed RGD circuit in Figure 11 with T_{D2} = 5 ns, 15 ns or 30 ns. When Q_3 is turned on, the inductor current, i_{L2} starts to charge to its maximum positive value defined from (26). After i_{L2} reaches its peak, it starts to decrease through $Q_{4,body\ diode}$, L_2, D_3 and V_{DD_in}. The process of i_{L2} is similar to i_{L1}. After the predetermined T_D, the MOSFET Q_4 will be turned on while Q_3 is off. i_{L2} will charge again but to a negative peak value, and starts to discharge to zero through the path of D_4, L_2, $Q_{3,body\ diode}$ and V_{DD_in}.

The circuit can also be explained in terms of energy processing. When Q_1 is turned on, energy is transferred from the power source, V_{DD_in} to the resonant inductor

and the gate capacitor. When V_{gs} of Q_1 reaches its peak, freewheeling of energy at inductor occurs. Then, the energy is returned to V_{DD_in}. Therefore, the proposed RGD demonstrates less power consumption compared to the conventional gate driver because of the energy recovery process.

The circuit also has the similar circuit operation for the discharging transition. When Q_2 is turned on, resonance takes place and the capacitive energy is transferred to the inductor. When i_{L1} starts to increase to the negative peak value, energy is merely freewheeling and finally, when the inductor current returns to zero, the inductor energy is also returned to the power source, V_{DD_in}. The circuit shows resemblance of symmetry of a conventional gate driver.

4.2 Proposed SBC Circuit

4.2.1 Operation of SBC Circuit

Referring to Figure 8, S_1 is the high side switch and it has the primary function of a buck converter, used to convert high input voltage into low output voltage indicated at the load. On the other hand, S_2 is the low side switch and it has a longer conduction time compared to S_1. The purpose is to lower the conduction loss in S_2. This statement can be verified by Table IV below.

Table IV Switching loss for varying duty ratio of S_2

Vgs,S_1 duty ratio, *D*	*Vgs*,S_2 duty ratio, *D*	S_1 Turn-off Peak (W)	S_2 Turn-on Peak (W)	S_1 Turn-off Switching Losses (W)	S_2 Turn-on Switching Losses (W)
25%	25%	91.617	109.726	1.603	2.195
25%	55%	87.060	98. 760	1.524	1.975
25%	72%	57.118	64.790	1.000	1.296
25%	73%	66.132	59.336	1.389	1.483

With the S_1 conduction time or duty ratio being constant, and S_2 duty ratio being varied, the results are plotted in line chart as shown in Figure 41.

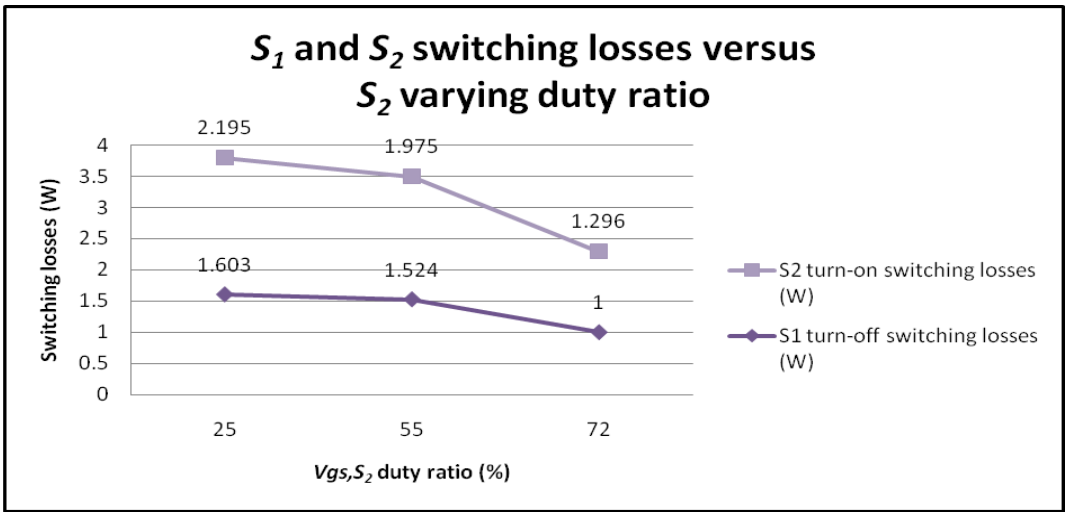


Figure 41 S_1 and S_2 switching losses versus S_2 varying duty ratio

From the results obtained, duty ratio of S_2 at 72% gives the lowest switching losses compared to other values. Therefore, it can be concluded that in order to reduce the conduction losses in the circuit, the conduction time of S_2 has to be at 72% optimized for low switching loss.

These 2 switches conduct complementary to each other. Since both of them are not turned on at the same time, cross conduction will not occur. During T_D, when S_1 is turned off, the discharged inductor current at the load will flow into body diode S_2, which is also at its off condition. ZVS can be achieved if S_2 is completely turned off before S_1 is turned on. During the Discontinuous Current Mode (DCM) operation, the negative load inductor current can be applied where the body diode of S_1 is turned on first before the main body of the switch itself. Therefore, the switching losses at S_1 can be reduced since it has experienced ZVS.

The operating waveforms of the proposed SBC circuit in simulation are shown in the Figure 42 below.

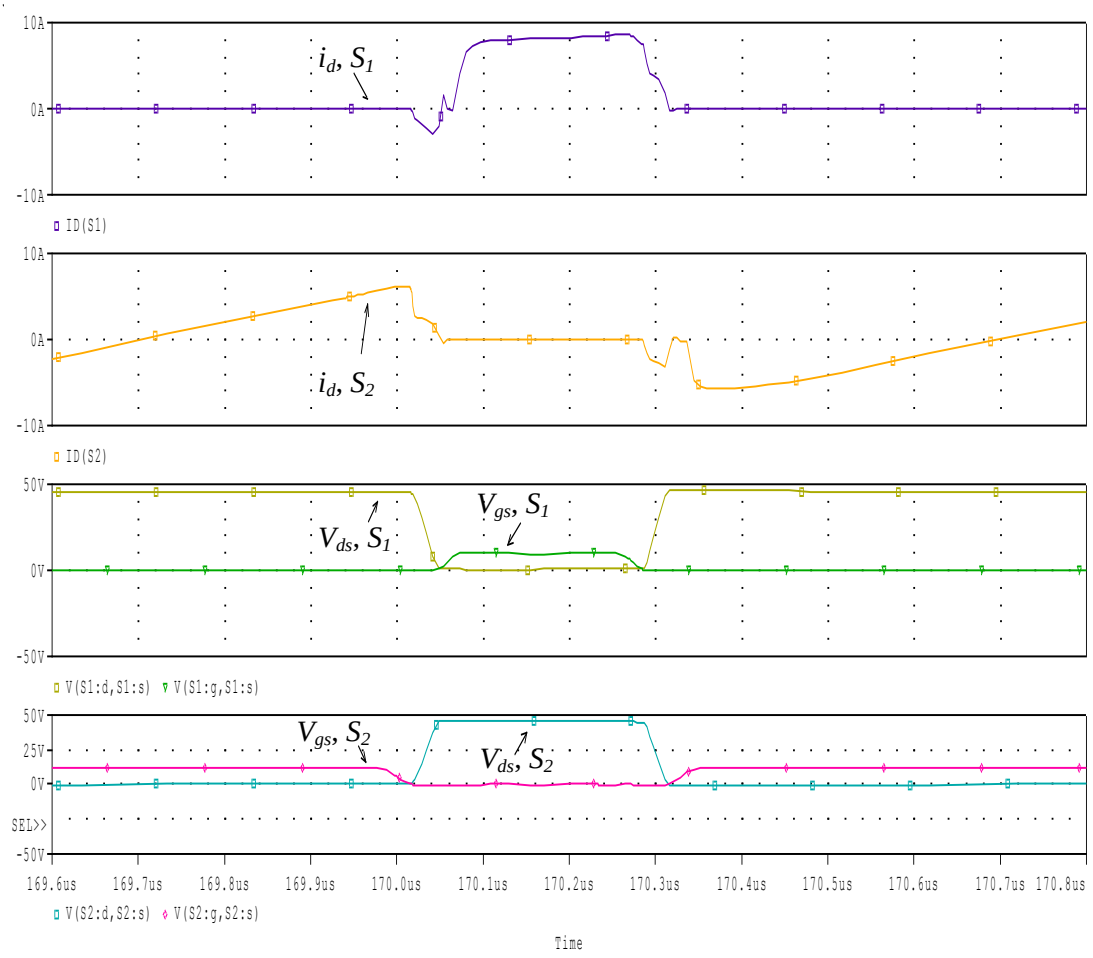


Figure 42 Operating waveforms of SBC Circuit

From the waveforms, the operation of SBC circuit starts when S_1 starts to conduct while $i_{ds,S2}$ at its peak value starts to decrease to zero and turn off. At this time, we can see that $V_{ds,\ S2}$ starts to increase to its maximum value which is the V_{in} value of 48 V while $V_{ds,\ S1}$ works in complimentary pattern and reduces to zero. The scenario of $V_{ds,\ S2}$ going to its peak value while $V_{ds,\ S1}$ goes to zero should happen at the same time, in other words, there is no time interval. This is because of freewheeling phase of $i_{ds,\ S1}$ [1]. It causes $V_{gs,\ S1}$ to go to zero first before $V_{ds,\ S1}$ reaches its maximum value. For the drain current of S_1, it can be observed that $i_{ds,\ S1}$ starts to increase exponentially to its highest value. At this moment, the conduction of $i_{ds,\ S1}$ circulates through L_s and C_s in the SBC circuit.

S_1 stops conducting when it reaches its highest point. But at this moment, S_2 does not conduct yet. This indicates a dead time exists when there is a change in conduction of switches. At this time, $V_{ds,\ S1}$ starts to increase while $V_{ds,\ S2}$ starts to decrease. On the other hand, $i_{ds,\ S2}$ starts to decrease to its maximum negative value whereas $i_{ds,\ S1}$ is at zero.

Following that, it can be seen from the figure $i_{ds,\ S2}$ starts to increase back to zero, which is like the previous state before it increases to its highest value while S_1 is off. At this moment, it can be observed that $i_{ds,\ S1}$ is at zero and $V_{ds,\ S1}$ is at its peak of the value V_{in}. This process repeats in the next subsequent cycles.

4.2.2 Calculating the switching power losses of SBC Circuit at T_D=15 ns

The power losses of the circuit are interpreted by generating the turn-off switching loss waveform of S_1 and turn-on switching loss of S_2 as shown in the figure below.

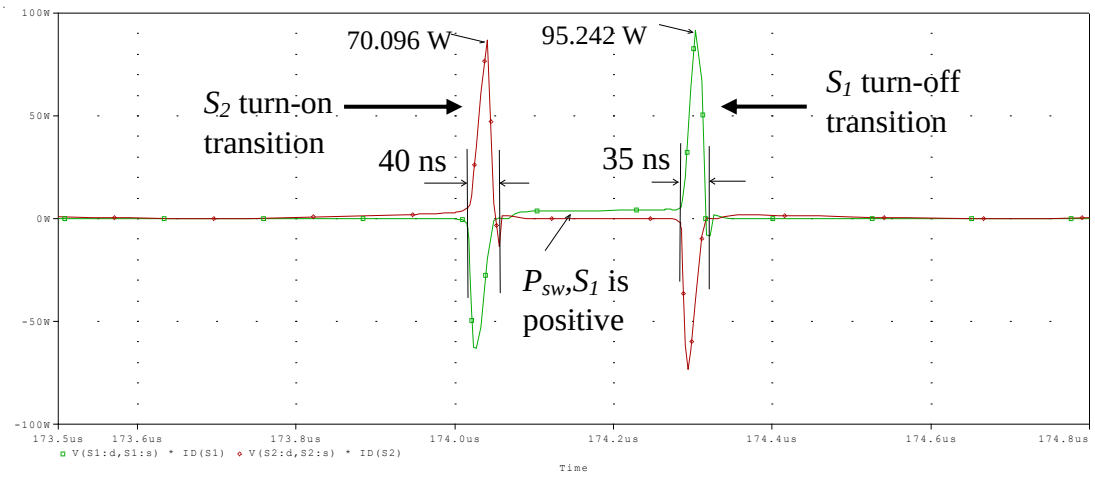


Figure 43 Turn-off switching loss of S_1 and turn-on switching loss of S_2

From the waveforms, the switching time for S_1 turn-off transition is 35 ns and for S_2, 40 ns. The calculation of switching losses is tabulated in Table V and the evaluated results are compared with [1].

Table V Comparing Switching losses from [1] and from this work

	From [1]	*From this work*	*% discrepancy*
S_1 Turn-off Peak V_{ds} * I_{ds}	*65.000 W*	*95.242 W*	*+ 31.8 %*
S_1 Turn-off Switching Losses 0,5*switching time*peak power*f_s	*1.138 W*	*1.667 W*	*+ 31.7 %*
S_2 Turn-on Peak V_{ds} * I_{ds}	*95.000 W*	*70.096 W*	*- 26.2 %*
S_2 Turn-on Switching Losses 0,5*switching time*peak power*f_s	*1.900 W*	*1.418 W*	*- 25.4 %*

From the table, the S_1 turn-off switching losses has increased by

$$\% \text{ loss increase at } S_1 = \frac{1.667 - 1.138}{1.667} \times 100\% = 31.7\ \%$$

While the S_2 turn-on switching losses has decreased by

$$\% \text{ loss saving at } S_2 = \frac{|1.418 - 1.900|}{1.900} \times 100\% = 25.4\ \%$$

From the results obtained, it can be observed that the turn-off switching losses of S_1 have increased. This is an unwanted case. The cause of this problem is the floating of $V_{ds,S1}$ which has caused the switching power loss to have a floating point too. This situation can be seen in the Figure 44.

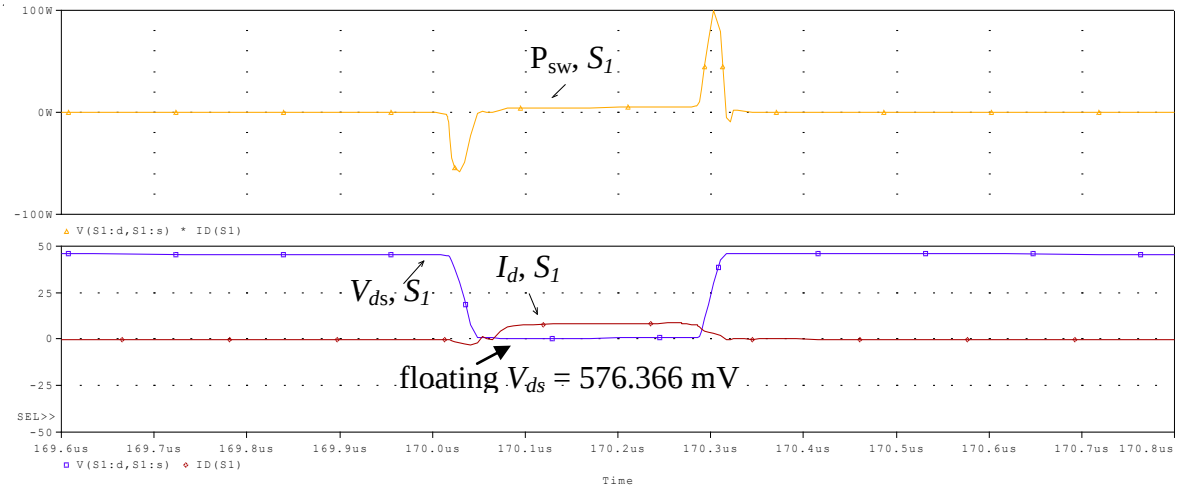


Figure 44 Floating point of $V_{ds,S1}$

It can also be observed that the positive peak is higher than the negative. This shows that the power losses are not equally distributed in S_1. In the circuit, S_1 is dominant in generating the power loss of the SBC circuit. Thus, L_s and C_s has been added to the circuit in parallel with S_1 to solve this problem. Meanwhile, C_x has also been added in order to prevent the floating drain voltage of S_1. Hence, theoretically, L_s, C_s and C_x have to be varied to reduce the switching losses at S_1.

On the other hand, S_2 turn-on switching losses have decreased by 25.4 % compared to the study in [1]. Figure 45 below shows the operating waveforms for S_2.

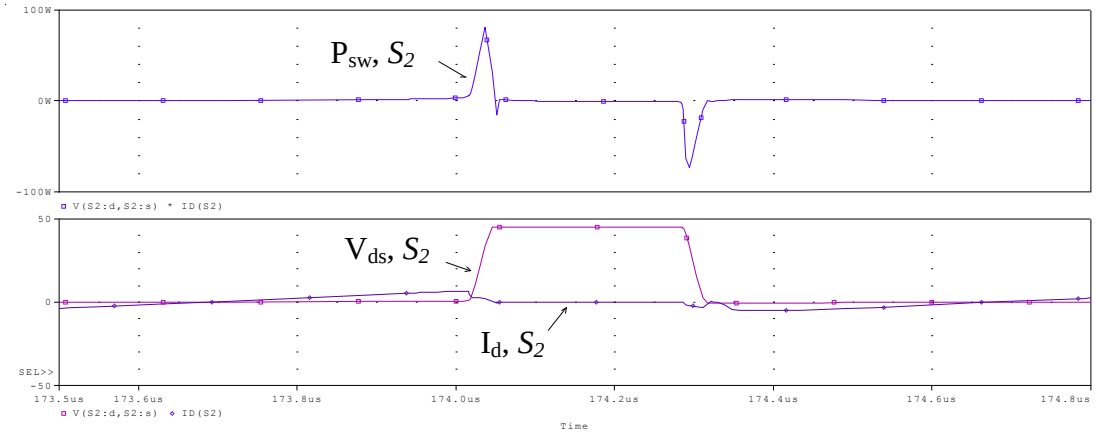


Figure 45 Operating waveforms for S_2

Compared to S_1, there is no floating point at V_{ds}, S_2. As expected there is reduction in the turn-on switching losses. And in return, the efficiency and reliability of the SBC circuit have improved.

4.2.3 Solving for increased switching losses at S_1

From simulation work, it is found that L_s gives the impact balancing the positive and negative peak and decreasing the switching losses at S_1.

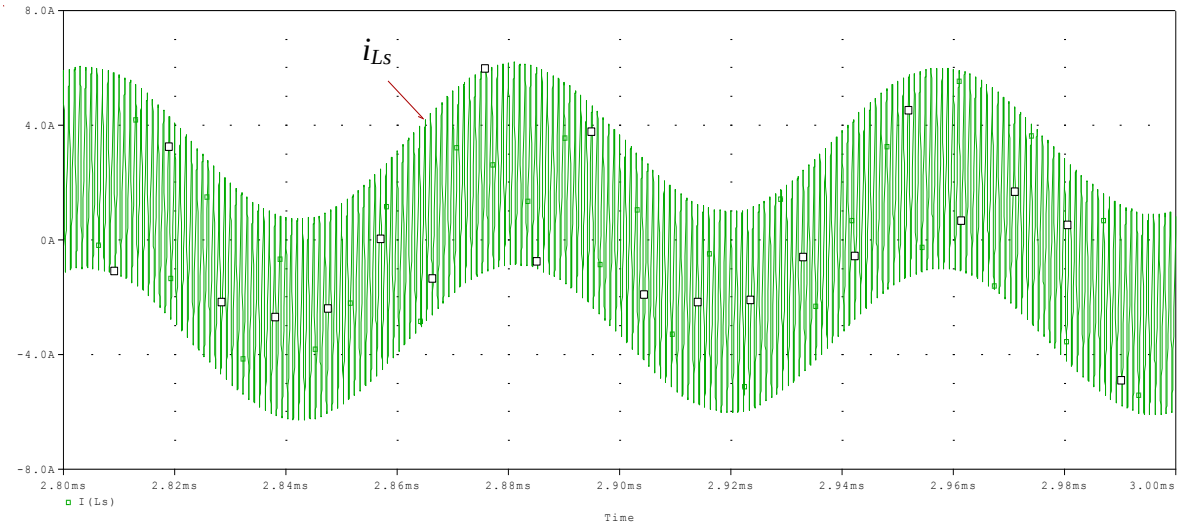


Figure 46 Waveform of i_{Ls}

Figure 46 shows the waveform of i_{Ls} and peak current shows a value of 6 A. The criterion of the component is that its maximum current must be at least 50 % more than the peak current conducted by L_s. Therefore, L_s must be able to conduct at least 9 A of current. According to the datasheet for component L = 1.2 μH with part number PM12639S, the maximum current that can be conducted is 21.0 A. Hence, it fulfills the criterion and can be applied to the circuit. The disadvantage of it is that, inductor with a higher inductance is more expensive compared to inductors with lower inductance.

The value of L_s is increased to 1.2 µH and the resulting waveform of S_1 and S_2 are shown in Figure 47.

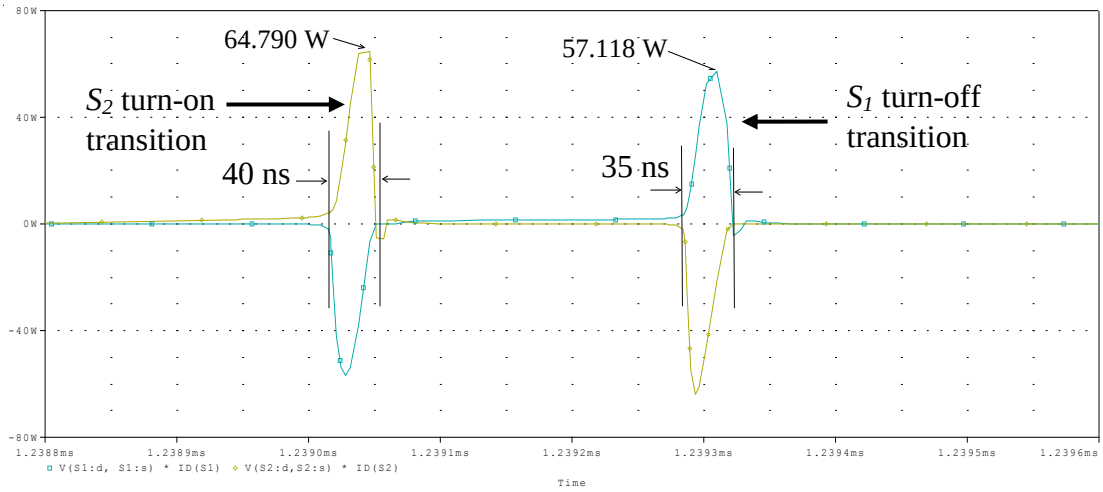


Figure 47 Switching loss of S_1 and S_2 with L_s=1.2 µH

From the results obtained, the switching losses of S_1 and S_2 are calculated again and tabulated in Table VI below.

Table VI Comparing switches losses from [1] and from this work with L_s=1.2 µH

	From [1]	*From this work with L_s=1.2 µH*	*% discrepancy*
S_1 Turn-off Peak V_{ds} * I_{ds}	*65.000 W*	*57.118 W*	*- 12.1 %*
S_1 Turn-off Switching Losses 0,5*switching time*peak power*f_s	*1.138 W*	*1.000 W*	*- 12.1 %*
S_2 Turn-on Peak V_{ds} * I_{ds}	*95.000 W*	*64.790 W*	*- 31.8 %*
S_2 Turn-on Switching Losses 0,5*switching time*peak power*f_s	*1.900 W*	*1.296 W*	*- 31.8 %*

The turn-off switching losses for S_1 have decreased by 12.1 % while turn-on switching losses for S_2 have further decreased to 31.8 %. The circuit has shown improvement and the primary objective of this work has been achieved.

4.3 Comparison of Circuit Performance for Several Values of Dead Time, T_D

4.3.1 Comparison of circuit performance in terms of power losses

This section discusses on the performance of the ZVS synchronous buck converter circuit for several values of T_D. With other parameter values remain unchanged except for T_D, and the overall performance of the circuit is analyzed. Table VII shows the circuit performance at T_D =5 ns, 15 ns, and 30 ns.

Table VII Comparison of circuit performance for varying values of T_D

T_D	V_{out} (V)	I_{out} (A)	t_{bd} (ns)	P_{cond} (W)	P_{bd} (W)	$P_{SW,S1}$ (W)	$P_{SW,S2}$ (W)	$P_{loss,total}$ (W)	P_{in} (W)	P_{out} (W)
5ns	14.061	1.4061	30	0.102	0.135	1.538	1.145	2.92	54.933	18.795
15ns	13.914	1.3912	33	0.100	0.1493	1.000	1.268	2.5173	56.020	19.188
30ns	14.155	1.4158	18	0.103	0.0816	1.707	1.823	3.7146	56.729	19.376

$P_{loss,total}$ is the total of all losses including conduction loss, P_{cond} from equation (19), body diode loss, P_{bd} from equation (20), and also switching losses, $P_{SW,S1}$ and $P_{SW,S2}$ as defined in equation (17) . From Table VII, it indicates that T_D at 15 ns gives the lowest total power loss, $P_{loss,total}$ of 2.5173W. By calculating the efficiency of the circuit at T_D=15 ns also gives the highest efficiency. Compared to T_D=5 ns and T_D=30 ns, T_D=15 ns is the most energy saving setting to be used. The switching losses, P_{SW} of the circuit are the major contributors of losses. P_{SW} comes from the two switches, S_1 and S_2, in the synchronous buck converter circuit. Theoretically, these losses can be reduced by reducing the switching time or peak power of both switches since P_{SW} =0,5*switching time*peak power*f_s. This means that the faster the MOSFETs can turn off, the more switching power can be reduced.

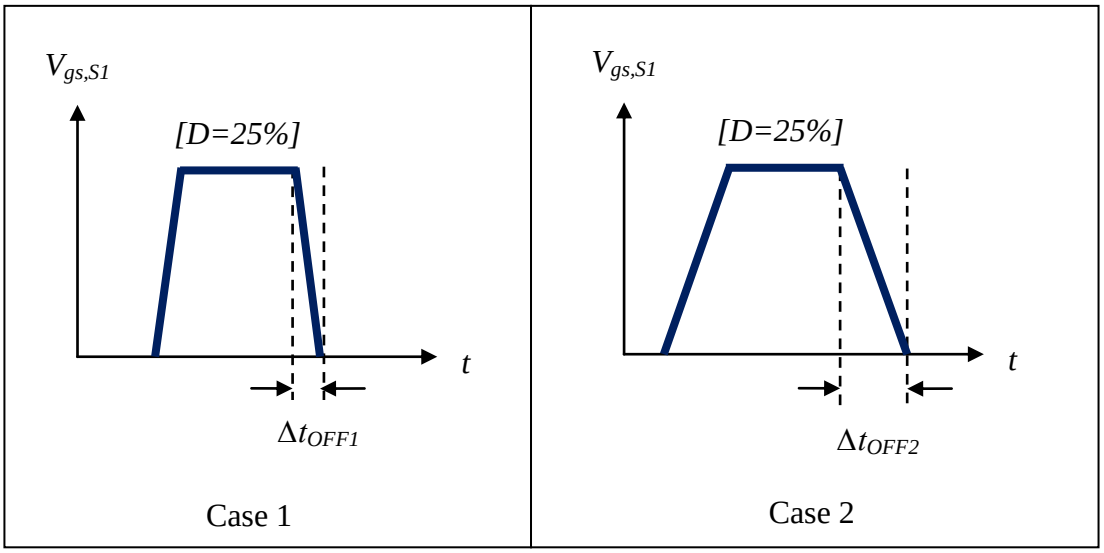


Figure 48 Varying the switching time of $V_{gs,S1}$

This statement can be proven by Figure 48 as the MOSFET $V_{gs,S1}$ of Case 1, Δt_{OFF1} turns off faster compared to $V_{gs,S1}$ of Case 2, Δt_{OFF2}. It can be seen that $\Delta t_{OFF1} < \Delta t_{OFF2}$. Therefore, the shorter the time taken for a switch to turn off, the more energy can be saved. This is because; a switch which has a smaller conduction time will produce less switching loss.

But as mentioned in the previous section, L_S also gives an impact on decreasing the P_{SW}. Therefore, in this work, several values of L_S are tested to get an optimum power loss in the two switches. This is shown in Table VIII.

Table VIII Total switching loss for varying value of L_s

Ls (uH)	Positive peak		Switching Time		S_1 turn-off switching losses (W)	S_2 turn-on switching losses (W)	Total switching loss (W)
	Switching loss of S1 (W)	Switching loss of S2 (W)	S_1 (ns)	S_2 (ns)			
0.9	95.242	70.096	35	40	1.667	1.402	3.069
1.0	94.038	58.273	38	44	1.787	1.282	3.069
1.1	61.694	71.383	35	40	1.080	1.428	2.508
1.2	57.118	64.790	35	40	1.000	1.296	2.296
1.3	55.375	61.607	40	42	1.108	1.294	2.402
1.4	55.601	55.306	40	45	1.112	1.244	2.356
1.5	53.695	55.465	42	50	1.128	1.387	2.515
2.0	47.294	44.399	52	61	1.230	1.354	2.584

From Table VIII, it can be concluded that total switching at L_s=1.2 uH, gives the lowest switching loss. The summary of the table is shown in the line graph of Figure 49.

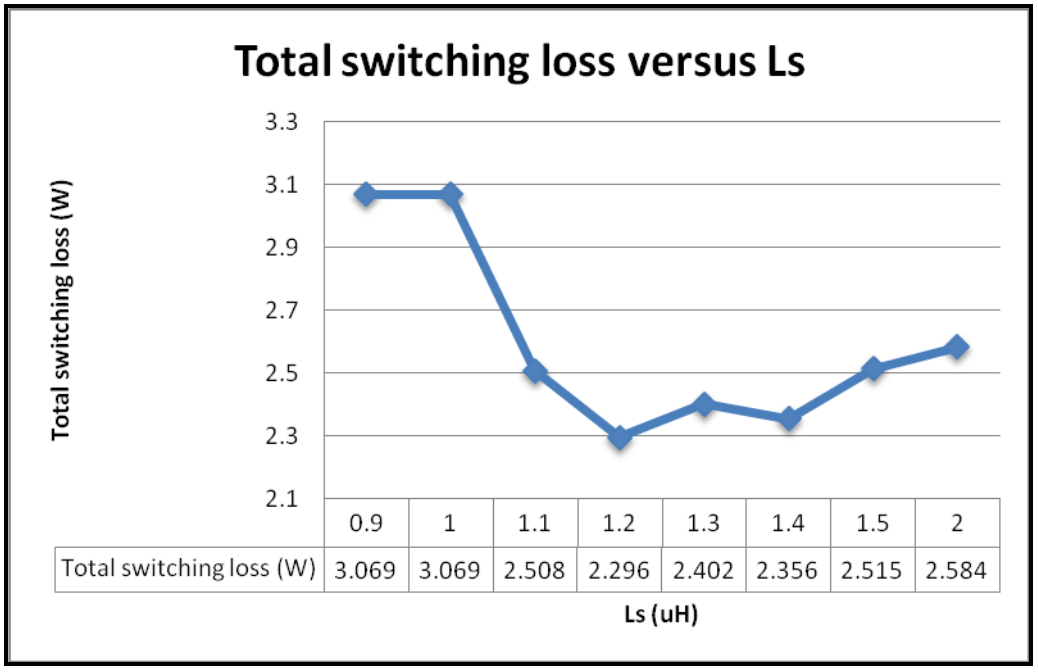


Figure 49 Graph of total switching loss versus L_s

4.3.2 Comparison of circuit performances in terms of steepness of slope

Table IX i_{L1}, peak time, rise time, recovery time and di_{L1}/dt of L_1 at several dead times

T_D (ns)	i_{L1} (A)	Peak time, t_{peak} (ms)	Rise time, t_{rise} (ns)	Recovery time, t_{rec} (ns)	di_{L1}/dt (A/ns)
5	3.2017	2.9700643	35.399	61.972	0.1238
15	3.3141	2.9700606	25.557	58.041	0.1727
30	3.0675	2.9700682	33.502	71.685	0.1223

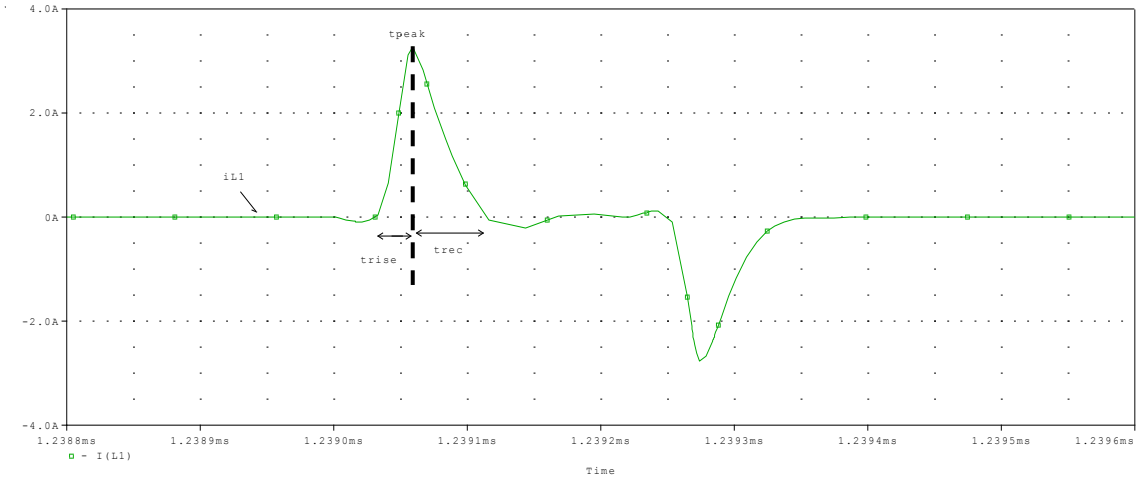


Figure 50 Inductor current, L_1 at T_D=15 ns

Table IX records the i_{L1}, peak time, rise time, recovery time and di_{L1}/dt at several dead times of inductor current of the left side RGD circuit. Figure 50 shows the measurement of peak time, rise time and recovery time of the inductor current. di_{L1}/dt is the rate at which inductor current changes with time. By differentiating the current, it actually gives the value of the steepness of the slope, which measures the speed of the circuit.

From the results tabulated, T_D at 15 ns shows the steepest slope compared to other dead times. It also shows the fastest rise time, t_{rise} as well as recovery time, t_{rec}. The importance of rise time is that, the faster the inductor current rises, the faster the circuit performance will be. On the other hand, recovery time means the time taken

for the energy to recover back in the gate driver of the circuit. If the time taken for the circuit to recovery the energy is shorter, the efficiency of the circuit would be higher. With the proposed RGD circuit, the charge and discharge current are constant and equal to each other. Therefore, switching time is reduced significantly and so does switching loss. Thus, it can be said that T_D = 15 ns shows better performance compared to other dead time.

Table X Rise time, fall time and *dv/dt* of S_1 and S_2 at several dead times

T_D (ns)	$t_{rise,S1}$ (ns)	$t_{fall,S1}$ (ns)	$t_{rise,S2}$ (ns)	$t_{fall,S2}$ (ns)	dv_{S1}/dt (V/ns)	dv_{S2}/dt (V/ns)
5	46.05	47.29	58.10	60.60	0.3538	0.7515
15	41.56	40.26	49.35	50.70	0.4039	0.7832
30	44.23	45.64	54.87	55.97	0.3812	0.6686

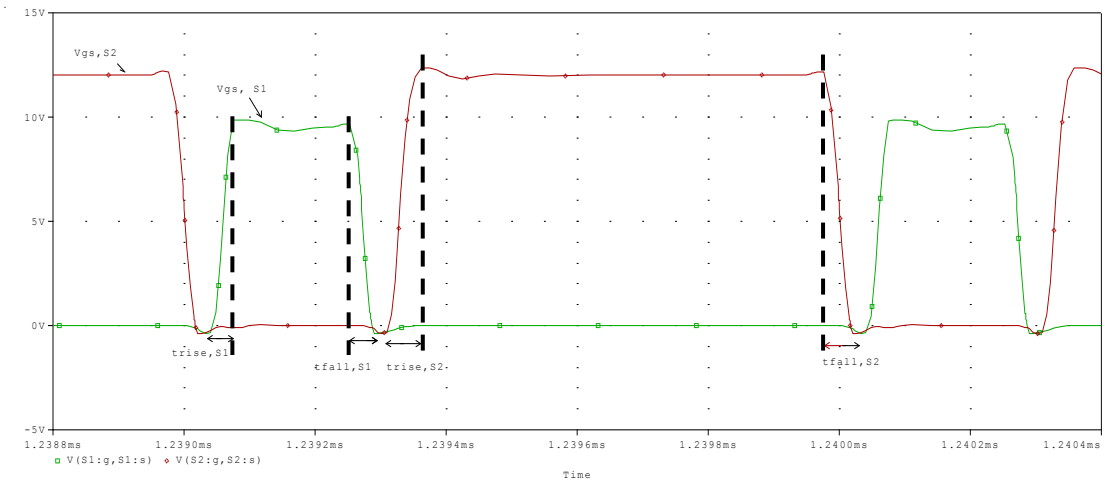


Figure 51 Inductor current, L_1 at T_D=15 ns

Table X shows the rise and fall times of both switches at SBC circuit while Figure 51 indicates the location of measurement. The table X above also includes the differentiation of V_{gs} of S_1 and S_2, dv_{S1}/dt and dv_{S2}/dt. Differentiation of V_{gs} indicates the steepness of the slope.

From the results obtained, again T_D = 15 ns shows the fastest rise and fall time for both switches. It indicates that the circuit gives better performance at this dead time. In terms of the gradient of the slope, the rising edge of V_{gs} is equal to the falling edge for both switches after simulation is done. A conventional SBC which does not possess this trait showing higher switching losses [1] compared to the SBC circuit used in this work. The voltage of $V_{gs,\ S2}$ = 12 V as it is clamped to the input voltage, also at 12 V.

4.3.3 Verification of results using Mathcad

Table XI Comparison of gradient values using PSpice and Mathcad

Parameters	Program		Difference	Percentage difference (%)
	PSpice	Mathcad		
Gradient of i_{L1} (A/ns)	-0.1000	-0.1295	0.0295	29.50
Gradient of $V_{gs,S1}$ (V/ns)	0.2377	0.2889	0.0512	21.54
Gradient of $V_{gs,S2}$ (V/ns)	-0.3716	-0.2800	0.0916	24.65

The results obtained in section 4.3.1. is compared with values obtained through the Mathcad program. By utilizing Mathcad, the formula for the function of either i_{L1}, $V_{gs,S1}$ or $V_{gs,S2}$ is written with reference to [10]. The constant variables are defined first. Then, using the X-Y graph plot function, the graph for i_{L1} is generated as shown in Figure 52.

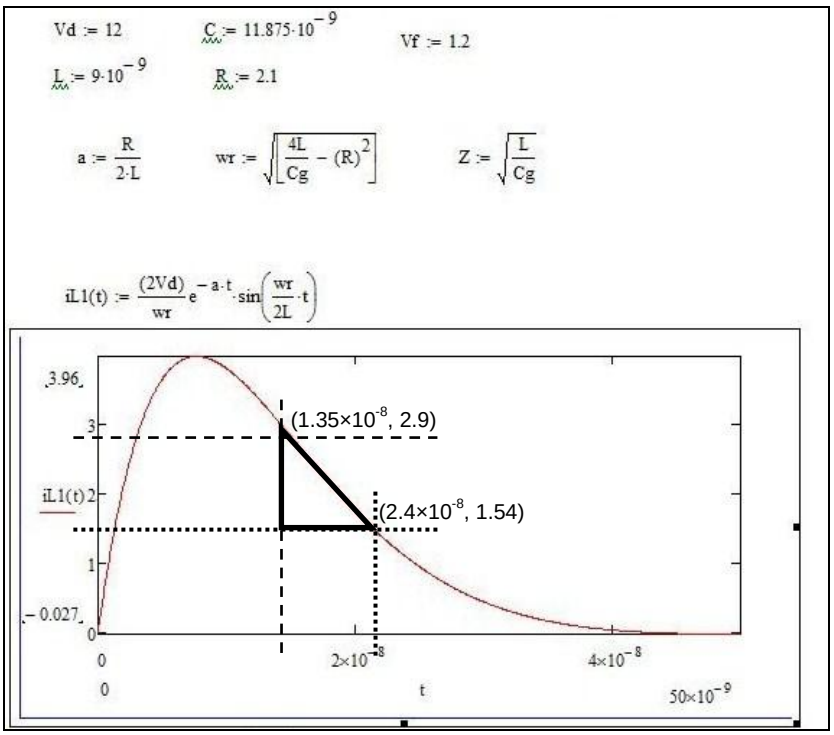


Figure 52 Graph of i_{L1} generated by Mathcad

Following that, the i_{L1} graph is also generated using PSpice program as shown in Figure 53. The gradient and the percentage difference of both graphs are calculated and compared as shown in Table XI. But note is taken that the peak current from calculation of Mathcad is at different values compared to the simulation values obtained. The reason is because initial current in simulation has not stabilized to its final value yet. Therefore, the gradient is calculated at 2.970 ms as shown in Figure 53. From the results obtained, the percentage difference is in between 10 % to 30 % which is considered as an acceptable range. Therefore, the results are verified.

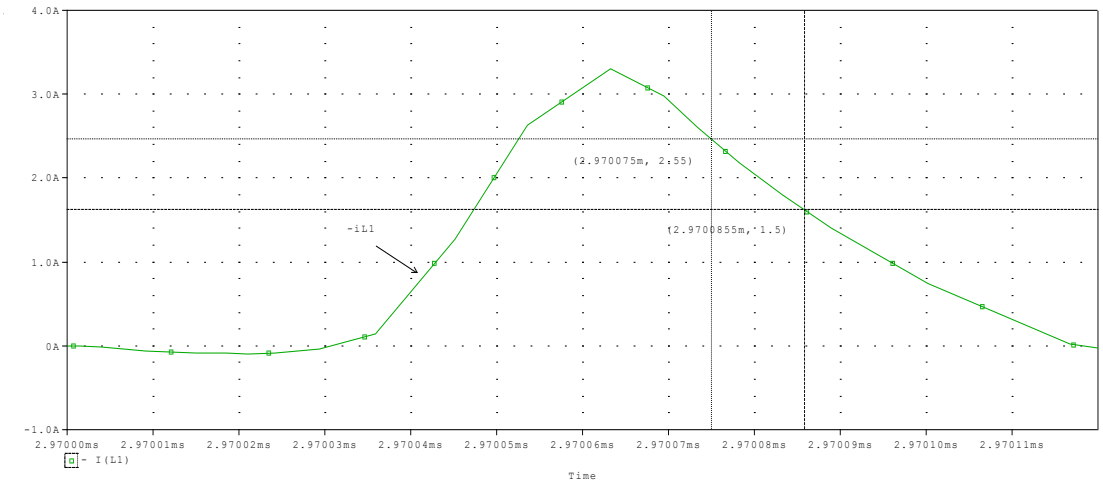


Figure 53 Graph of i_{L1} generated by PSpice

4.3.4 Verification of results using formula calculation

Table XII Comparison of results from formula calculation and PSpice

Parameters	Method		Difference	Percentage difference (%)
	Formula	PSpice		
Rise time, t_r (ns) equation (27)	25.810	25.557	0.253	0.98
Recovery time, t_{rec} (ns) equation (28)	51.620	58.041	6.421	11.06
Peak current, $i_{L1}(t_{peak})$ (A) equation (29)	3.572	3.367	0.205	5.74
Total switching loss, $P_{sw,total}$ (W) equation (18)	2.517	2.517	0.000	0.00
Conduction loss, P_{cond} (W) equation (19)	0.100	0.100	0.000	0.00
Body diode loss, P_{bd} (W) equation (20)	0.149	0.149	0.000	0.00

Utilizing Mathcad, equations (27), (28) and (29) are used to obtain the theoretical values. The results are then compared with the values obtained using Pspice from section 4.3.2. The comparison is shown in Table XII.

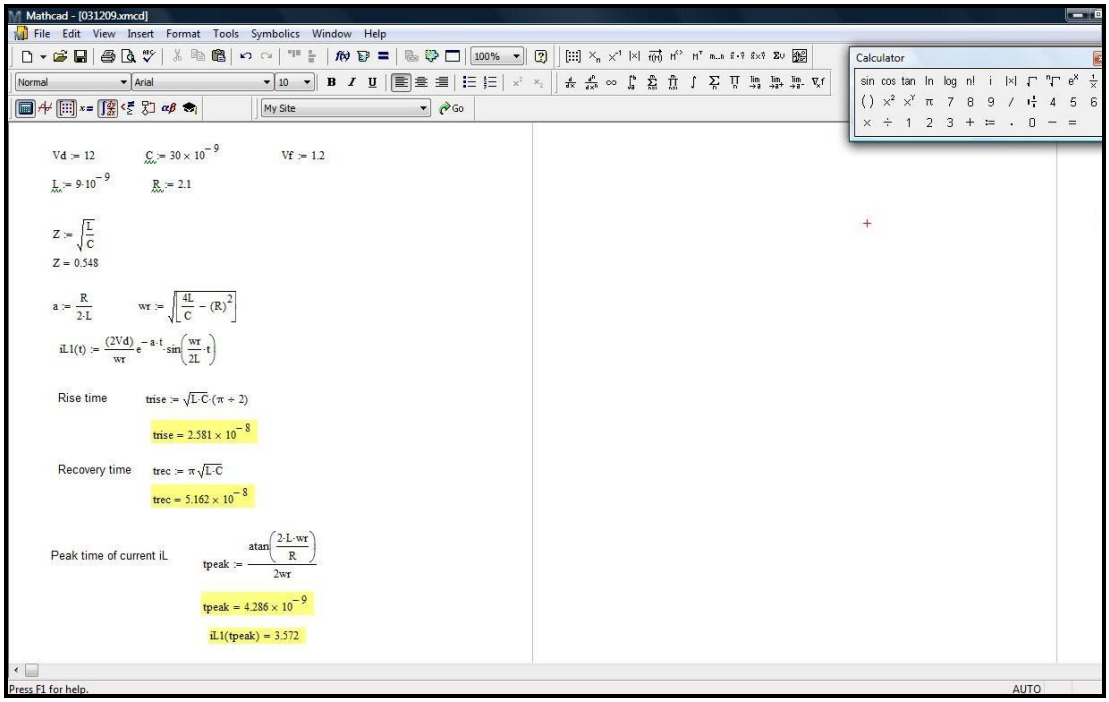
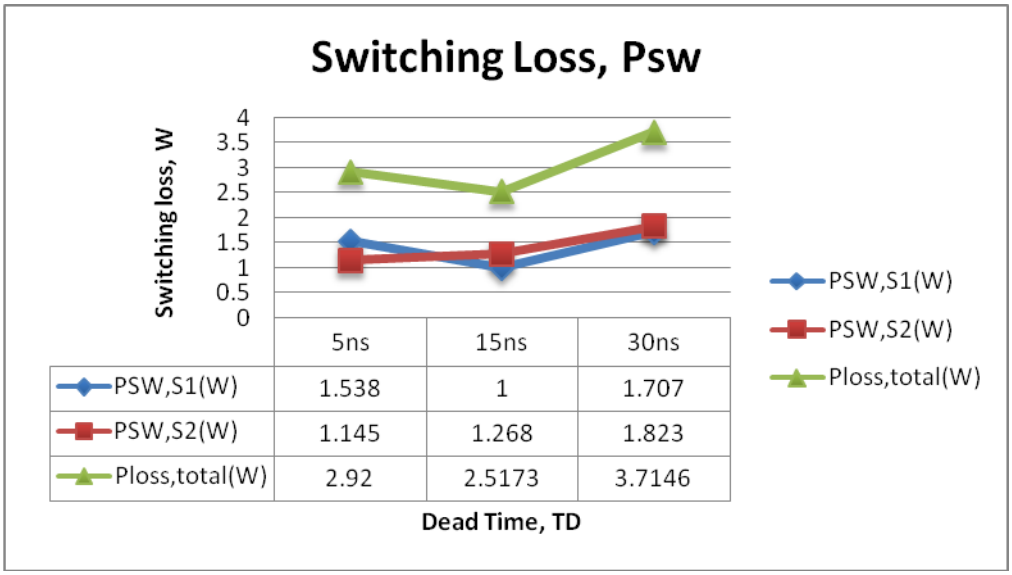


Figure 54 Results generated by Mathcad using formulas

Figure 54 shows the definition of variables and formulas used in Mathcad to obtain the values of Table XII. The percentage difference is then calculated. The difference between the results obtained from PSpice and by calculation from the formulas is at a considerable range of 0% to 12%. The results are acceptable and verified.

4.3.5 Comparison of circuit performance using graph representation

Different variables from Table VII are compared by using graph to represent the data.



	5ns	15ns	30ns
PSW,S1(W)	1.538	1	1.707
PSW,S2(W)	1.145	1.268	1.823
Ploss,total(W)	2.92	2.5173	3.7146

Figure 55 Switching loss at different dead time

Figure 55 shows relationship between switching loss at S_1, $P_{SW,S1}$ and switching loss at S_2, $P_{SW,S2}$ with respect to dead time, T_D. Switching loss of switches in the circuit is more dominant compared to conduction loss, P_{cond} and body diode loss, P_{bd}. From the graph shown, the switching losses at both switches are not proportional to each other. S_1 indicates the least switching loss at T_D = 15 ns, while S_2 indicates the least switching loss at T_D = 5 ns.

The factor that affects the switching loss is V_{ds} where body diode conduction time, t_{bd} and the voltage amplitude plays an important role. Both body diode conduction for T_D = 5 ns and 15 ns are generated as shown in Figure 56 and 57.

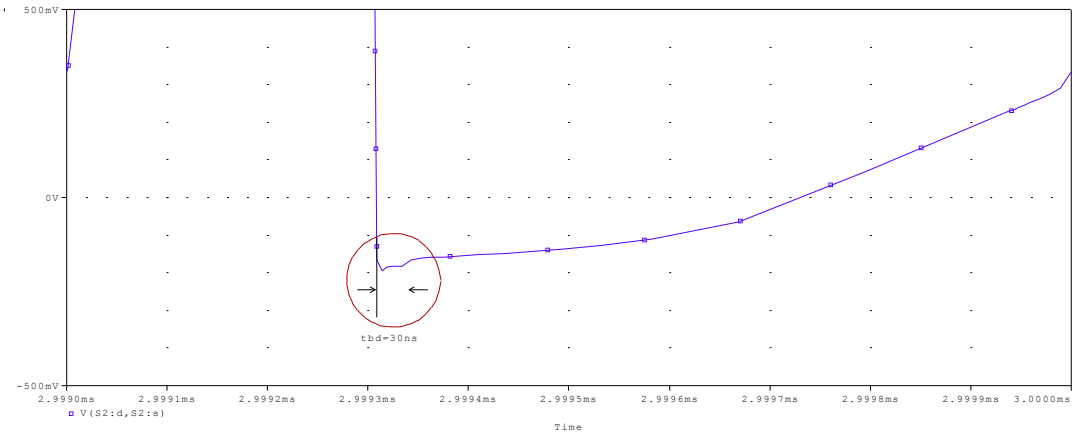


Figure 56 Body diode conduction time of S_2 at T_D=5 ns

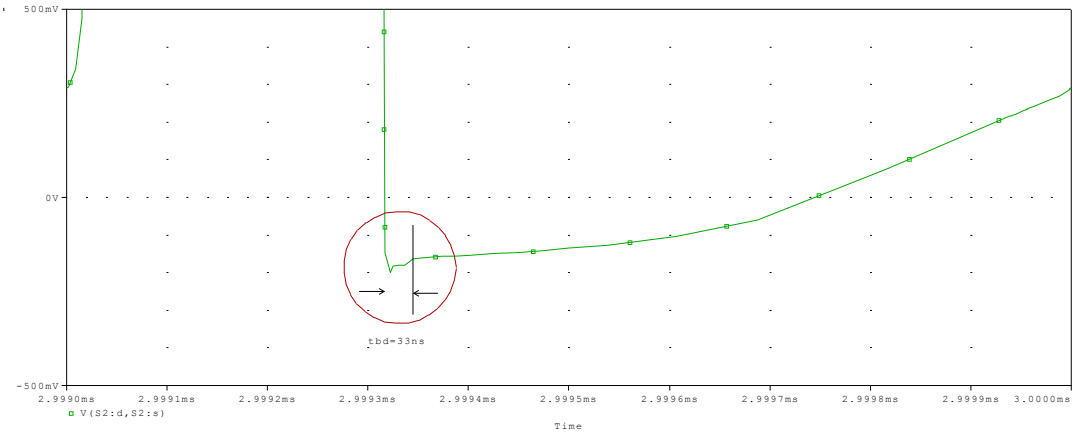


Figure 57 Body diode conduction time of S_2 at T_D=15 ns

Figure 56 shows t_{bd} =30 ns while Figure 57 shows t_{bd}=33 ns. The longer body diode conduction time is (T_D = 15 ns) the higher switching loss at S_2 will be. Figure 55 verifies the relationship of t_{bd} with the $P_{SW,S2}$. Body diode conduction is an undesirable factor in any circuit because it contributes to higher switching loss.

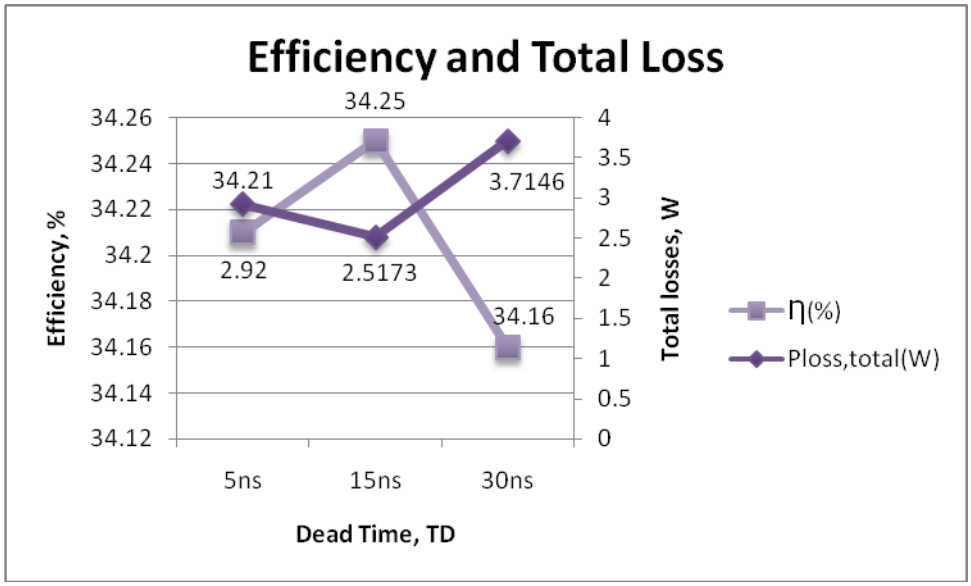


Figure 58 Relationship between Efficiency and Total Loss against Dead Time, T_D

Total power loss, $P_{loss,\ total}$ is inversely proportional to the efficiency, η of the circuit defined in equation (14). As $P_{loss,\ total}$ increases, the circuit will be less efficient and vice versa. The synchronous buck converter circuit shows the highest efficiency of 34.25 % at T_D = 15 ns because of the least $P_{loss,\ total}$ of 2.5173 W.

The efficiency of 34.25 % is basically not high enough. The factor that affects the efficiency is output power, P_{out} and input power, P_{in}. From the results obtained, P_{in} has a larger effect on the efficiency compared to P_{out}. Therefore, P_{in} has to have a lower value in order to increase the efficiency of the overall circuit.

The simulation results presented in this section demonstrate that with the proposed RGD circuit at T_D =15 ns, the power loss can be reduced, and therefore, improve the efficiency.

CHAPTER 5
CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

In conclusion, switching losses in converter circuit are present due to high and low side switches operating in high frequency system. The gate driver circuit plays an important part in activating these switches. In order to reduce the losses, the dead time and duty ratio of the RGD circuit can be adjusted. The PSpice software is used to implement this project.

The simulation of the circuit using PSpice has been carried out. Waveforms from the proposed RGD circuit as well as the proposed SBC circuit have been generated and interpreted. Following that, the switching loss graph is obtained and the switching losses for both S_1 and S_2 are calculated and compared to the findings from [1]. It has shown a decrease in losses by 12.1 % in S_1 and 31.8% in S_2, respectively. Besides that, the total power loss is obtained for T_D =5 ns, 15 ns and 30 ns. Verification of the graphs has been made utilizing Mathcad program. All the results have been tabulated along with the values of P_{in} and P_{out}. Analysis and comparison of the circuit performance is also made and it can be concluded that T_D =15 ns is the optimum value for the best circuit performance.

5.2 Recommendations

For future work, it is recommended that the circuit be implemented onto hardware to verify the simulation results obtained.

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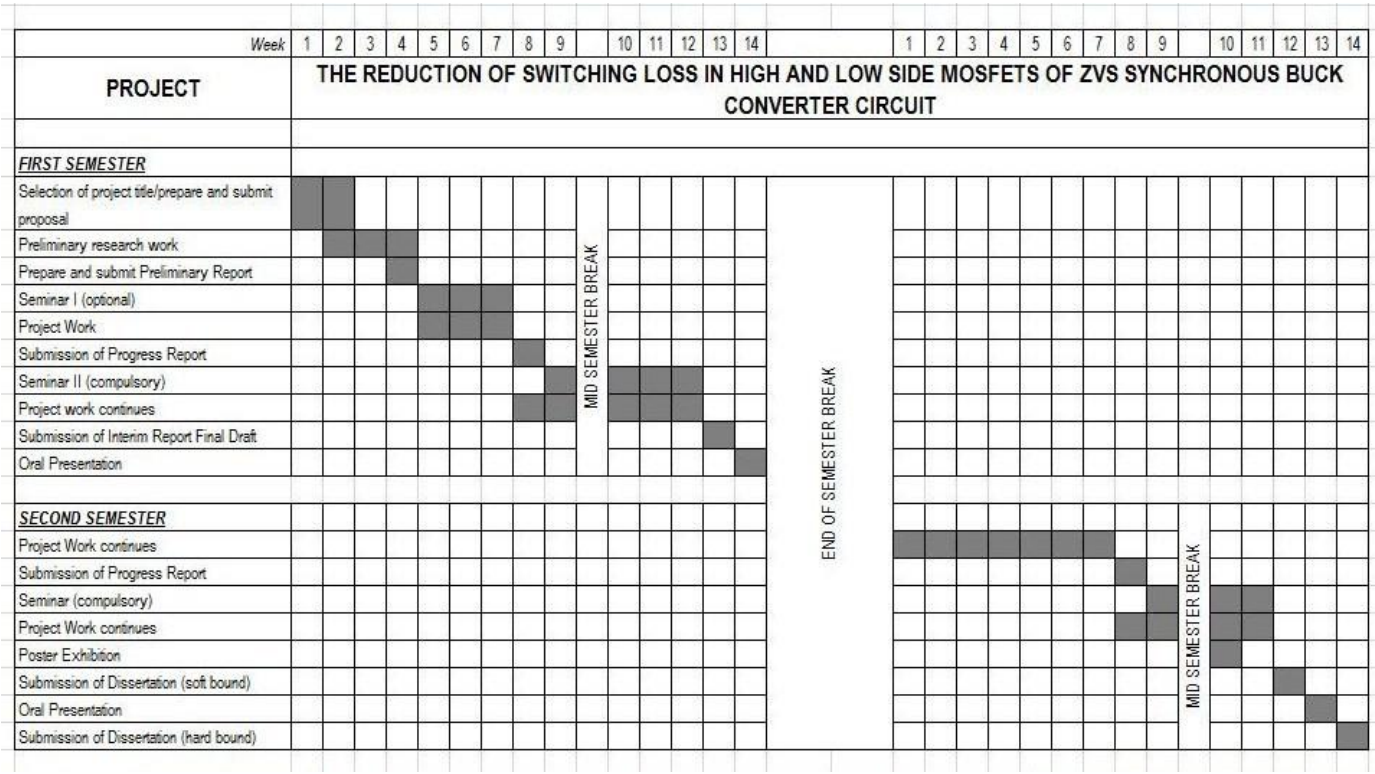
APPENDICES

APPENDIX A

GANTT CHART



APPENDIX B

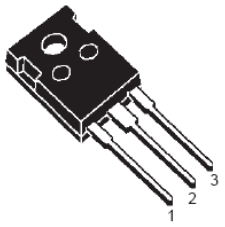
IRFP250 DATASHEET

IRFP250

N-CHANNEL 200V - 0.073Ω - 33A TO-247
PowerMesh™ II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP250	200V	< 0.085Ω	33 A

- TYPICAL $R_{DS}(on)$ = 0.073Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED



TO-247

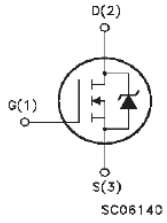
DESCRIPTION

The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UNINTERRUPTIBLE POWER SUPPLIES (UPS)
- DC-AC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	33	A
I_D	Drain Current (continuos) at T_C = 100°C	20	A
I_{DM} (●)	Drain Current (pulsed)	132	A
P_{TOT}	Total Dissipation at T_C = 25°C	180	W
	Derating Factor	1.44	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤33A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.66	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	33	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	600	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 16A		0.073	0.085	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	33			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 16A	10	25		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2850		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			120		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 100V, I_D =16 A		25		ns
t_r	Rise Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		50		ns
Q_g	Total Gate Charge	V_{DD} = 160V, I_D = 33 A,		117	158	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V, R_G = 4.7Ω		15		nC
Q_{gd}	Gate-Drain Charge			50		nC

SWITCHING OFF

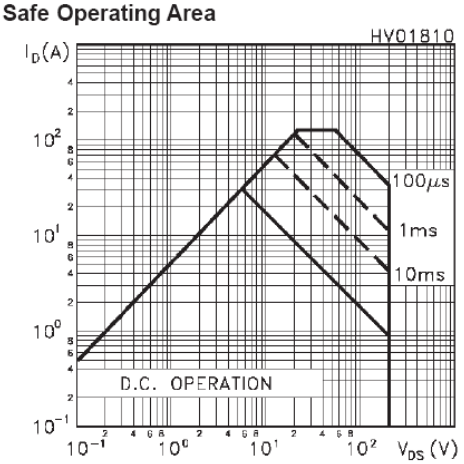
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160V, I_D = 16 A,		60		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		40		ns
t_c	Cross-over Time			100		ns

SOURCE DRAIN DIODE

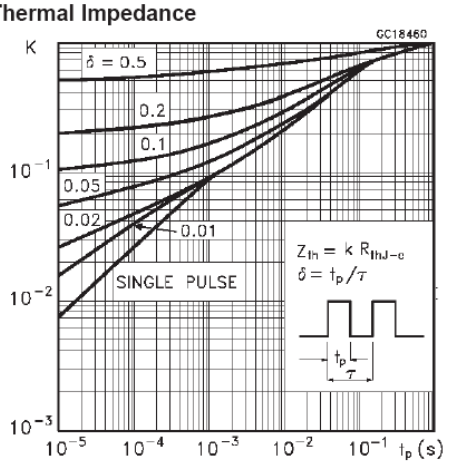
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				33	A
I_{SDM} (2)	Source-drain Current (pulsed)				132	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 33 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 33 A, di/dt = 100A/µs,		370		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		5.4		µC
I_{RRM}	Reverse Recovery Current			29		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

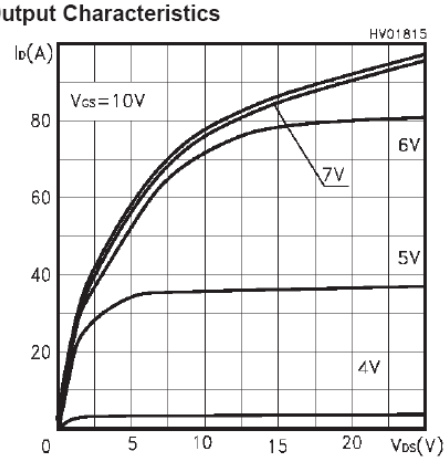
Safe Operating Area



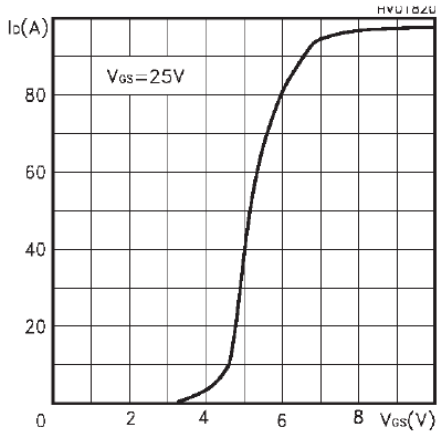
Thermal Impedance



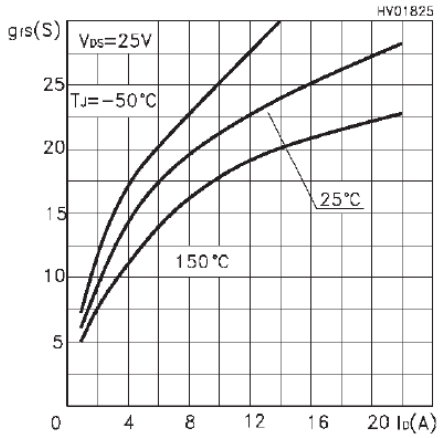
Output Characteristics



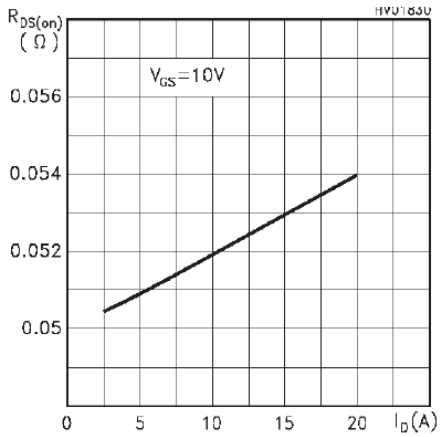
Tranfer Characteristics



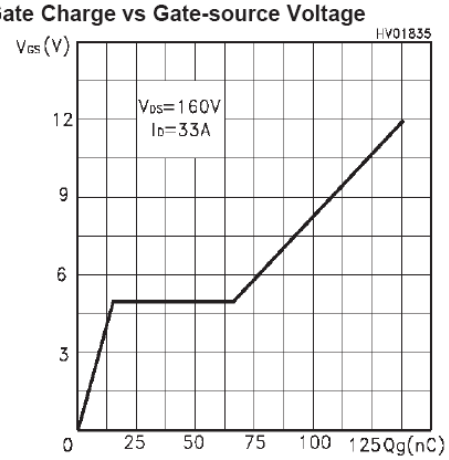
Tranconductance



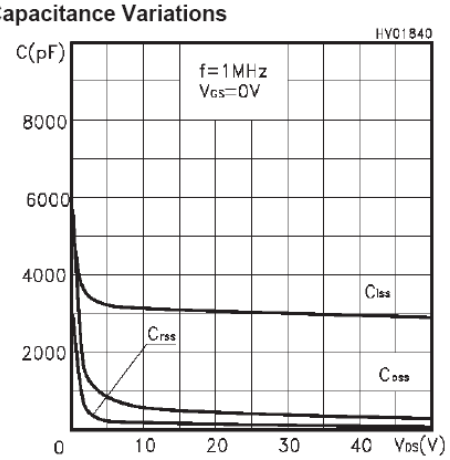
Static Drain-Source On Resistance



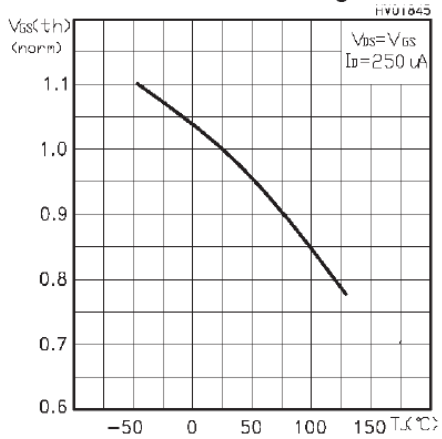
Gate Charge vs Gate-source Voltage



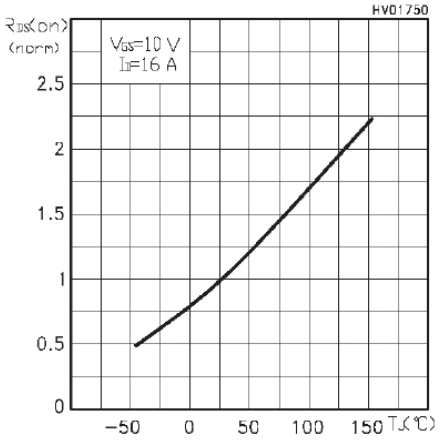
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

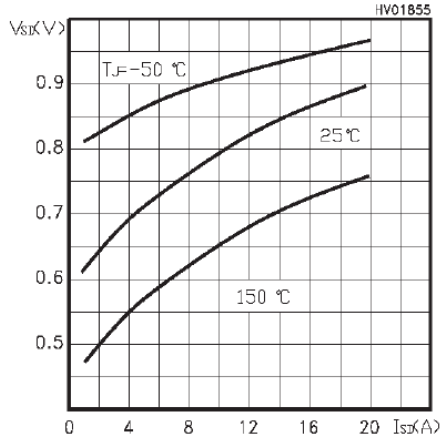


Fig. 1: Unclamped Inductive Load Test Circuit

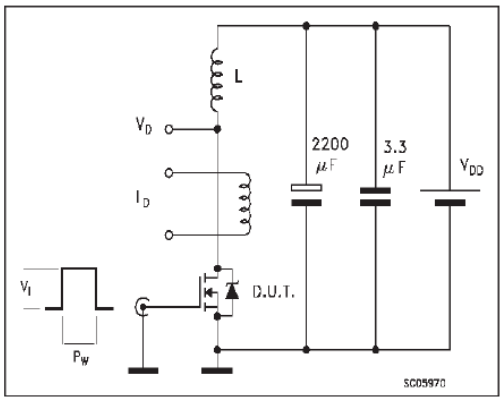


Fig. 2: Unclamped Inductive Waveform

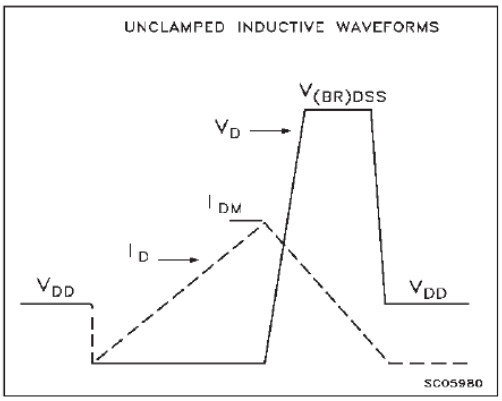


Fig. 3: Switching Times Test Circuit For Resistive Load

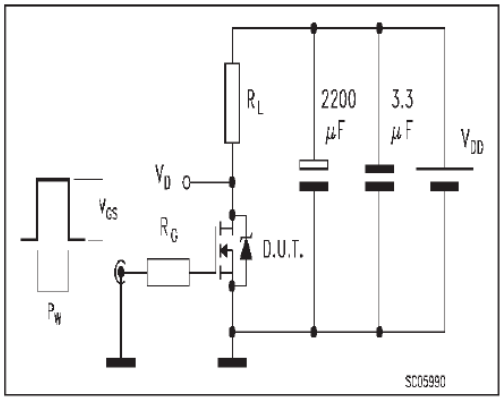


Fig. 4: Gate Charge test Circuit

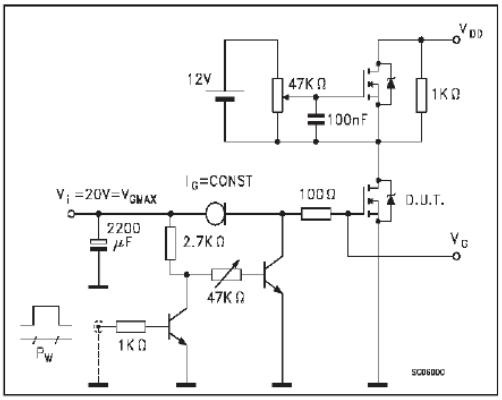
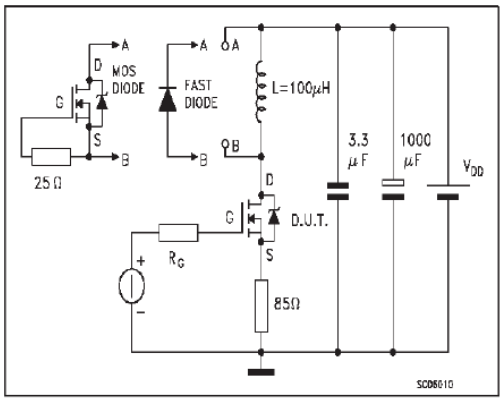


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118